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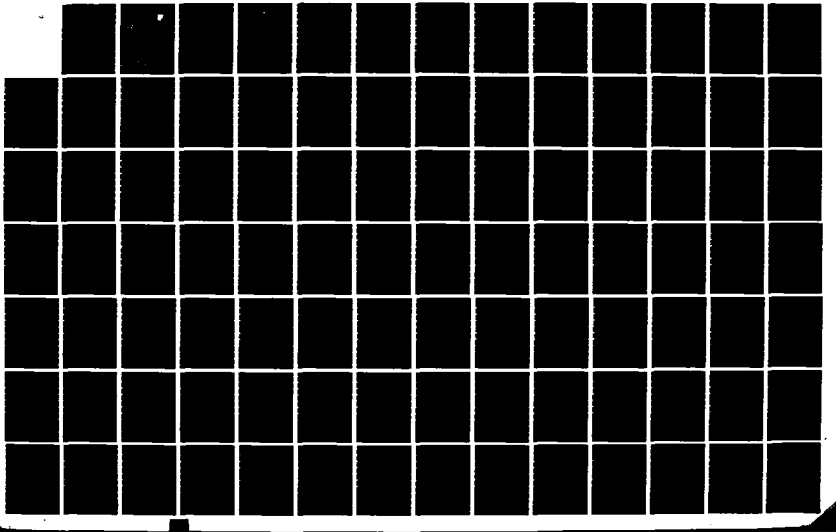

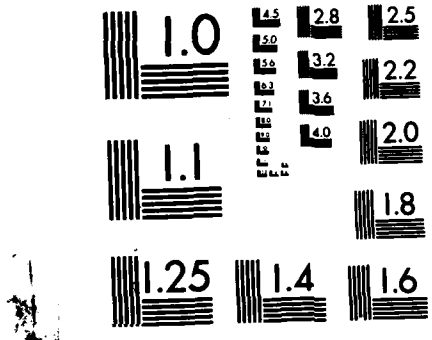

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TESTABILITY OF VLSI LEAKAGE FAULTS IN CMOS

State University of New York at Binghamton

Yashwant K. Malaiya and Stephen Y. H. Su

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With the advent of VLSI (Very Large Scale Integration), the importance of CMOS (Complementary Metal Oxide Semiconductor) technology has increased. CMOS offers some very significant advantages over NMOS, and has emerged very competitive. Therefore, testability of CMOS devices is of considerable importance.

CMOS devices exhibit some failure modes which are not adequately represented by the classical stuck-at fault model. A new fault model is introduced

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here to represent such faults. Leakage faults are specifically examined in this report, such faults increase the static supply current (which is ordinarily quite low) substantially. A leakage testing experiment consists of applying different vectors to the circuit, and in each case measuring the static supply current. This experimentally obtained data is then analyzed to obtain fault-related information. Leakage testing offers extra testability without any additional pins. It can detect some faults which cannot be detected by the conventional testing.

Test generation for several basic CMOS structures is considered. Correspondence between leakage testing and conventional testing is studied.

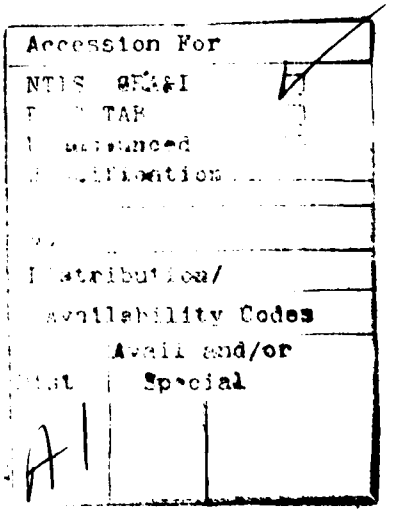
Two methods for analyzing experimental data are presented. Available experimental data was analyzed to obtain statistical information. Such statistical information can be used to devise efficient test generation and information extraction methods. The study indicates leakage testing is feasible and is a potentially powerful tool for testing CMOS VLSI.

EVALUATION

This work has provided a key link in establishing the possibility of designing completely testable integrated circuits. The restrictions of such designs to classic CMOS without transmission gates, which is required at the present state of knowledge is known now to be a sufficient condition. It is not yet known to be a necessary condition, and that portion which requires not using transmission gates is thought to be unnecessary.

It is problematic as to whether the semiconductor industry has the capability for producing parts which would have a sufficient yield when subjected to testing and selection according to the limits which complete testability would require. In particular, the supply leakage current limits in all states would have to be severely reduced, causing many parts to be rejected for leakage currents which would probably not be functionally significant in and of themselves but which would pose the risk of masking the presence of another fault which was a functional or reliability hazard.

MARK W. LEVI



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I. INTRODUCTION

The VLSI era brings a new set of testing problems. Testing has been relatively easy for SSI and MSI devices. The simple stuck-at-fault model worked very well; it was easy to generate tests and determine their effectiveness. Integration on the larger scale presents problems. There can be an extremely large number of possible states, and to control a node and to observe it, long sequences of operations are required. Accessibility of nodes can be increased. This, however, generally requires additional pins, a very significant price to pay. It is also being recognized now tht the classical stuck-at-0, stuck-at-1 fault model is sometimes inadequate. The resources and the effort required to test the newer devices are enormous. The testing of VLSI devices has therefore assumed great significance.

The CMOS devices, until recently, have not been as common as bipolar or NMOS. This was inspite of the fact that they offer several significant advantages over other technologies [1.1]:

1. CMOS devices offer the best noise immunity for magnetically-coupled noise. It is typically 45% of the logic swing; the theoretical maximum for binary devices is 50%. This is because of the very sharp transfer characteristic for CMOS structures [1.2] as shown in Fig. 1.1.
2. CMOS rise and fall time are about equal.
3. For a given patterned gate line width, CMOS is about twice as fast as NMOS.

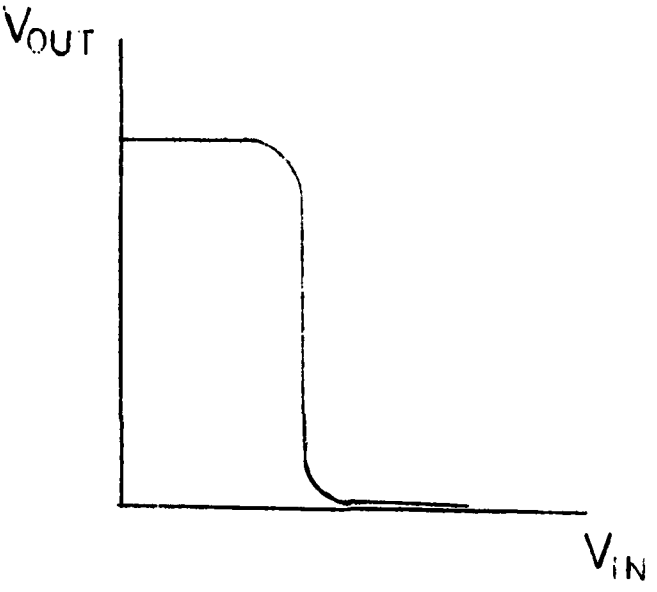

Fig. 1.1: CMOS transfer characteristic.

4. CMOS devices can use supply voltages in a range of magnitudes.
5. Perhaps most importantly, the CMOS static power consumption is very small. This is because in a static situation, a CMOS gate never has a direct (low resistance) current path across V_{DD} and V_{SS} terminals.

In Fig. 1.2, a basic two inputs CMOS NOR gate is shown. For a P-channel (N-channel) transistor to conduct, it is necessary that a relatively negative (positive) voltage (exceeding the threshold value) be applied to the gate, so that a channel is induced. Consider the four possible cases listed below:

I1	I2	Non-conducting (off) transistors
0	0	N1,N2
0	1	N1,P2
1	0	P1,N2
1	1	N1,N2

In all four cases there is never a low resistance path between V_{DD} and V_{SS}. An OFF transistor offers extremely high resistance, and only a small leakage current (of the orders of a few nanoamperes) flows, as is discussed later.

The CMOS devices had been more expensive, because they involve more components and until recently more processing steps. The situation has now changed in favor of CMOS [1.3].

1. High performance N-channel wafer costs are converging to CMOS wafer costs.

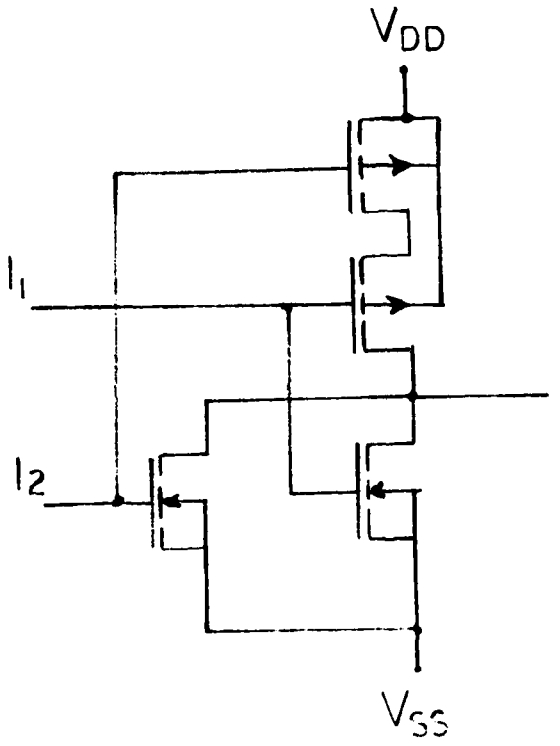

Fig. 1.2: A two-input CMOS NOR gate. The substrate and the P-cell connections are also shown.

2. CMOS layout density is approaching N-channel.
3. CAD device and circuit simulation programs are less complex for CMOS than NMOS, because CMOS uses only enhancement transistors.
4. For VLSI devices, even N-channel technology will have heat dissipation problems; CMOS can therefore achiev .igher densities.

Testing of CMOS devices is therefore of special imp c :e. The concerns also arise because CMOS can exhibit failure modes, which are not considered in classical testing.

A new approach for testing CMOS devices is considered here. It has been a practical observation, that the static supply current (also referred as leakage current) is very sensitive to faults and marginalities in the chip. Very high leakage currents are observed in cases when a chip has a fault or is soon to develop a fault. Various aspects of testing via measurement of leakage currents are considered.

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II. FAILURES IN CMOS DEVICES

A basic CMOS block is made up of two parts, one consisting of only P-channel FETs and the other containing only N-channel FETs connected in a complimentary manner. For every P-channel transistor, PA, which is in series (parallel) to another P-channel transistor, PB, there is a corresponding N-channel transistor, NA, which is in parallel (series) to another N-channel transistor, NB. Thus in contrast to NMOS structures, the single depletion N-channel load is replaced by a complementary network of P-channel transistors (Fig. 2.1).

Although the complementary structure requires more transistors, it imparts the device two very desirable characteristics. First is that the voltage transfer characteristic is symmetrical, and has a sharp drop, giving high noise immunity. Secondly, because in a static situation, the structure always presents a very high resistance across the supply terminals V_{DD} and V_{SS}. Only when the device is switching, momentarily there is low resistance path and appreciable current flow.

For the enhancement FET to conduct, it is necessary that a channel should be induced. For V_{DS} (drain to source voltage) about zero, it is necessary that the magnitude of V_{GS} should exceed a certain value, V_T, called the threshold voltage. The resistance of a conducting transistor in CMOS devices is very low, of the order of a few ohms. A conducting transistor will be referred to as ON in the following discussion.

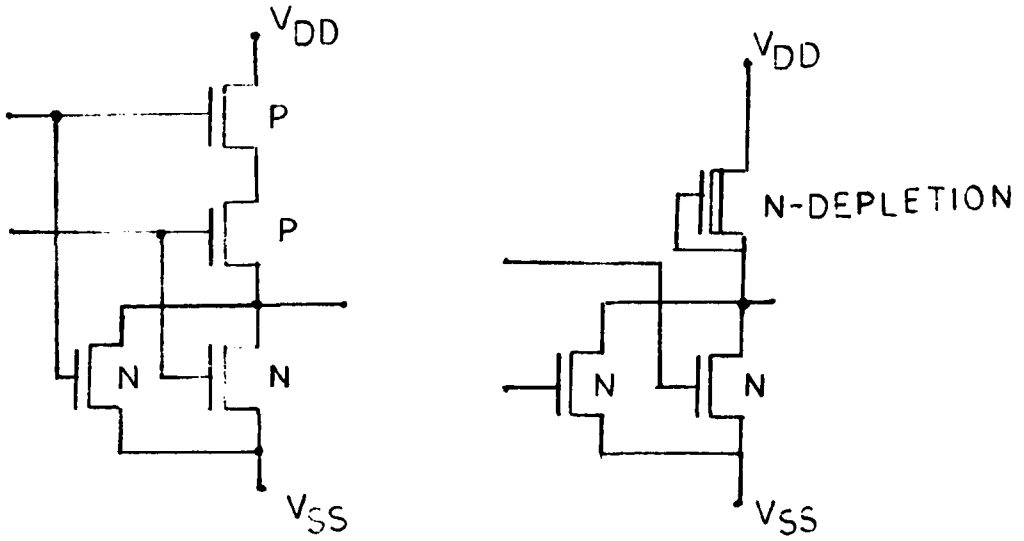


Fig. 2.1: CMOS and NMOS NOR gates.

A non-conducting transistor (OFF) ideally offers infinite resistance. However, if there is a significant V_{DS} present (it can be almost equal to $V_{DD}-V_{SS}$), a very small drain to source current, called leakage current, can flow through it. For normal transistors the leakage current arises because of two components. One part is because of the surface currents which depend on surface contamination and crystal-plane orientation. As both contamination and circuit geometry cannot be very precisely controlled or measured, this leakage current cannot be exactly predicted, but useful limits can be found by empirical methods. The other component current is the bulk leakage current due to the reverse currents of the P-N junctions. Temperature and voltage relationships of this are well understood [2.1]. This, however, may be insignificant compared to the surface current component. It can be expected that for identical V_{DS}, and temperature, the transistors on a single chip will have about the same leakage current. This was confirmed by our analysis of data, as will be seen later. Even though the leakage current for a transistor varies somewhat from chip to chip, this is not a severe problem, as small variations in a comparatively small quantity (compared with abnormal leakage currents) are not very significant.

The gate leakage current can be of the order of 10^{-15} Ampere [2.2]. This is insignificant compared to drain to source leakage current. We can, therefore, assume that the isolation of the gate from the rest of the transistor is ideal.

The causes of failures in MOS and CMOS devices have been extensively studied [2.3]. Some of the significant physical failure

mechanisms in CMOS are [2.4]:

--Open circuit, with a transistor or interconnection.

--Short circuits.

--Threshold drift because of surface contamination.

The following failure modes causing logical faults are possible [2.5]:

1. Open or short transistor.
2. An open input to a gate causing the input to drift to a S-a-1 or S-a-0 condition (undefined).
3. An open gate transistor causing that device to drift to a permanent open or short condition. Electrically this is equivalent to mode 1.
4. Shorts between gate inputs or shorts from input to output.

The faults may be classified into overlapping classes according to the manner in which they can be modelled:

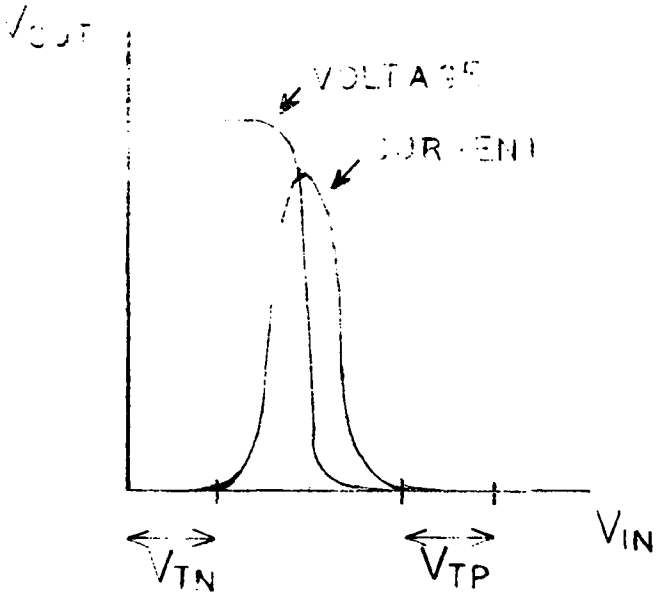
1. Several failure modes can be modelled as gate inputs or output stuck-at-1 or stuck-at-0. The classical methods, which assume this stuck-at fault model, have worked well, and standard techniques and software packages are available for them. However, some important failure modes cannot represented by stuck-at fault model, and methods to handle are needed. The inadequacy of stuck-at fault model in CMOS devices has recently become a subject of investigation.
2. Short between lines will require electrical consideration before the effect of the short can be determined. Investigations

have been done for such faults, based on the assumption that the effect can be logically represented as an AND or an OR operation. It can be easily seen that the assumption may not always be valid. For CMOS devices, the voltage at a shorted pair of nodes will depend on the total effective resistances connecting them to the V_{DD} and V_{SS} lines. There, can be another important effect. If two nodes are shorted, and if logical values are such that the two nodes would otherwise have opposite logical values, then very high supply current will result. This is because in CMOS nodes with logical 1 are connected through a low resistance path to V_{DD} and nodes with logical 0 are connected through a low resistance path to V_{SS}. If nodes with otherwise opposite logical values are shorted, then there will exist a low resistance path between V_{DB} and V_{SS}, drawing high supply current.

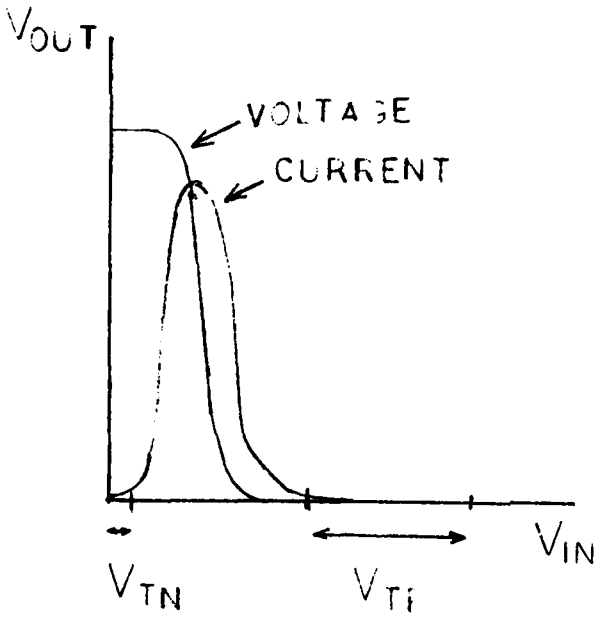
3. Some faults can be modelled as open or short transistors. These were termed as stuck-open and stuck-on faults by Wadsack [2.6]. The effect of some of them can be modelled as stuck-at 0 and stuck-at 1 faults, but not always. Such faults (specially stuck-open) have recently received some attention from testing and simulation point of view. Wadsack had suggested techniques for simulating stuck-open faults by using then existing simulators. The newer simulators [2.7, 2.8] can simulate them in more direct fashion. The stuck-open faults can cause combinational elements to display sequential behavior, because capacitances can hold the earlier logic values. Elzig [2.7]

and Elzig and Cloutier [2.8] have shown that stuck-open faults in CMOS gates and complex cells can be tested by applying stuck-at test vectors (generated for stuck-at 0 and stuck-at 1 faults) in a specific order. Chiang and Vranesic [2.9] have considered test generation for stuck-open and stuck-on transistors by using graphical considerations.

In MOS, another important class of faults is possible. Some faults can cause excessive leakage current to flow. Such faults may or may not affect the logical operation. In the latter case, they are likely to be harbinger of eventual logical failures. The faults, which will be referred to as leakage faults, can cause leakage current which can be several orders of magnitude more than the normal value. This can cause significantly higher power consumption and localized heating can cause faster aging of related area on the chip. One cause of leakage faults is threshold drift due to migration of alkali ions [2.3]. Threshold drift causes the threshold voltage of P-channel transistors to increase and N-channel transistors to decrease. As shown in Fig. 2.2, this causes the transfer characteristic to shift to the left, allowing significant supply current to flow. When the drift has advanced sufficiently, the output voltage can no longer exceed $(V_{DD}-V_{SS})/2$; when the input is V_{SS}, hence gets effectively stuck-at 0.



(a) No threshold drift.



(b) Some threshold drift.

Fig. 2.2: Effect of threshold drift.

In this report a new fault model is presented which can model leakage faults, as well as some other important failure modes. The significance of testing for leakage faults is considered in the next section.

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III. MOTIVATION

There are several motivations for investigating a leakage current based testing technique.

1. Extra testability generally requires extra components, especially extra pins. Extra pins are a very significant overhead. They can significantly increase the cost of the integrated circuit. Extra pins may also reduce the reliability, as both within and outside a chip, the number of pins is related to the unreliability. The leakage testing technique provides extra test data (information), but uses only already existing V_{DD} and V_{SS} pins [3.1].

2. In conventional testing, test generation for a specific fault consists of two steps. First the site of the fault has to be excited, and then effect of the fault has to be propagated to the external outputs. In leakage testing, the propagation of the effect of the fault is automatic, as the excessive leakage current is sensed at the supply terminals V_{DD} and V_{SS}.

3. The conventional testing provides gate level resolution. Leakage testing can give transistor-level resolution.

4. As it is considered in the next section, several important types of faults can be modelled as leakage faults. Some faults like those caused by threshold drift can be detected by leakage testing even before they start affecting the logical operation.

5. Monitoring supply current is a very effective method for testing of shorts. If the two nodes which otherwise would have had

posite logical values are shorted, then a very high supply current ll flow because of the low resistance path created.

6. As it is explained below, some shorted transistors may not fect any logical operation, and hence cannot be tested by conventional esting. Such faults are easily detected by leakage testing.

7. The excessive leakage current is generally a few orders of agnitude greater than the normal leakage current. Excessive leakage s therefore easily identifiable.

8. Leakage testing can ensure that opens are not masked during pen's test, as suggested by Levi [3.1].

9. Besides being harbinger of eventual logical failures, excessive eakage itself is very undesirable. It can represent power consumption few orders of magnitude higher than expected or allowed for in a lesign. In applications where power is supplied by limited overall capability (like in a space mission), this can significantly reduce the mission time.

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IV. THE CONDUCTANCE FAULT MODEL

The conductance fault model introduced below models switching and resistivity of the transistors. Since the model represents the static behavior, capacitances are not needed. As will be clear from the following discussion, it is more convenient to use conductance rather than resistance to characterize transistors. The model is based on these facts:

--An ON transistor has very high conductance (very low resistance) of about 10^{-1} ohm^{-1}.

--An OFF transistor can be represented by a leakage conductance. Ideally its value is 0 (infinite resistance); practically a normal transistor has a leakage conductance of the order of 10^{-12} ohm^{-1}. For an abnormal (leaky) transistor it can assume a value of 10^{-9} or higher.

--The gate is well isolated from the channel. Therefore, a transistor presents only a single path, from drain to source, for the leakage current.

The model is represented in Fig. 4.1. It has an ideal switch which inserts either the ON conductance or the OFF conductance in the supply current path between V_{DD} and V_{SS}.

In the normal case, the ON conductance is very high and the OFF conductance is very low. We can now consider two possible situations for faulty behavior.

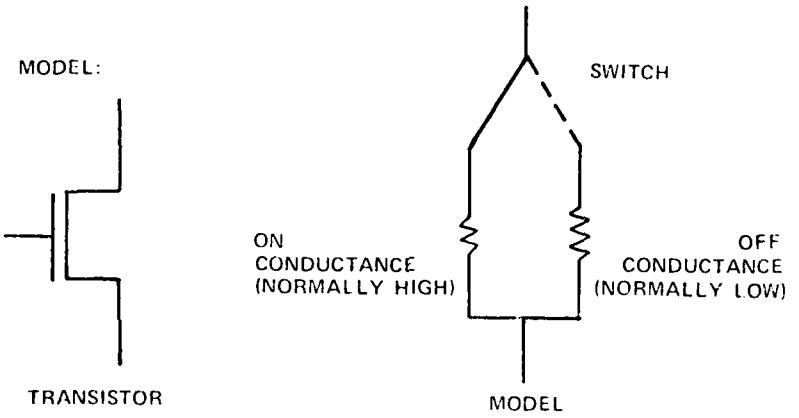

Fig. 4.1: The conductance fault model.

1. The ON conductance can be too low. This corresponds to the situation when the path between V_{DD} and V_{SS} is open. This corresponds to stuck-open faults.
2. The OFF conductance can be too high. This will cause an excessive leakage current whenever appropriate V_{DS} ($V_{DS} = V_{DD} - V_{SS}$) is present. We term this a leakage fault. In the extreme case, when the abnormal OFF conductance approaches normal ON conductance, it corresponds to the stuck-on faults.

The stuck-open and stuck-on faults can occur in both MOS and CMOS devices. They were first identified by Wadsack [4.1]. Test generation for them has been considered in [4.2, 4.3, 4.4], simulation [4.1, 4.5, 4.6] and testable design in [4.7]. Only the leakage faults are considered in this report.

Because of its simplicity, the conductance model is suitable for simulation. If dynamic behavior is also desired (for example, for handling the sequential behavior of stuck-open faults), appropriate capacitances have to be added.

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V. TESTING BY MEASURING LEAKAGE CURRENT

The leakage current in CMOS is controlled by the OFF transistors with appropriate voltage across them. By applying different input vectors to combinational circuits (input and state vectors for sequential circuits) different sets of transistors can be made to control the overall supply current. One can, therefore, measure the supply current under different vectors and then extract some information about the transistors from the data.

Example 1: Consider the NAND gate shown in Fig. 5.1. To keep the explanation simple, let us assume that the integrated circuit chip does not contain anything else. The overall conductance of the chip under each vector can be measured by measuring the supply current and dividing it by the supply voltage. If the OFF conductances of transistors NA, NB, PA, PB are represented by C(NA), C(NB), C(PA), C(PB), and if the measured conductances under input vectors 00, 01, 10, 11 are indicated by C_0, C_1, C_2, C_3, respectively, then the following conductance equations are obtained.

Vector		Unknowns	Measured Values
A	B		
0	0	$[C(NA)^{-1} + C(NB)^{-1}]^{-1}$	$= C_0$
0	1	$C(NA)$	$= C_1$
1	0	$C(NB)$	$= C_2$
1	1	$C(PA) + C(PB)$	$= C_3$

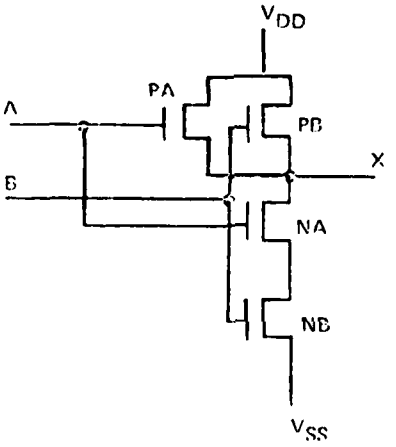

Fig. 5.1: NAND gate for example 1.

We thus obtain a set of equations where conductances of different transistors are unknowns. In the above set, values of C(NA) and C(NB) are given immediately. Since transistors PA and PB are in parallel, there is no way to distinguish between C(PA) and C(PB), and thus C(PA) + C(PB) should be treated as a single variable. The first equation is dependent on the rest and hence provides only redundant information.

After the conductances of different transistors or groups of transistors in parallel are obtained, it can be checked if they are less than a specified value. If the conductance of a transistor is greater than the maximum allowed, it can be regarded as faulty. Because of restricted experimental accuracy, the lower bound of acceptable range can neither be defined nor used.

The above procedure, which can be called equation-solving method, can easily be applied to individual NAND, NOR and inverter gates, as well as their fanout-free networks. In general, however, several problems are encountered.

--Nonlinear terms may be involved, these will make solving the set of equations difficult to automate.

--If all possible vectors are used, a large number of equations are obtained. The equations are not, in general, linearly independent. After the redundant equations are removed, there might be fewer equations than variables. It is still possible to extract information from these equations. The equations can be considered as constraints and maximum and minimum values of variables can be obtained.

Transistors with minimum conductance values more than allowable maximum are definitely leaky. Those with maximum conductance values, less than allowable maximum, are definitely normal. However, all this would require large computation time. An alternative way is to use set-theoretic methods based on probabilistic aspects of the problem.

VI. CONSIDERATIONS ON TEST GENERATION

Like in conventional testing, test generation for leakage testing require two considerations. First is to sensitize the fault so that its effect can be examined. In leakage testing, a transistor is sensitized if it is OFF, and its terminals are connected to V_{DD} and V_{SS} through low resistance paths. If the transistor is leaky, it will present a low resistance path between V_{DD} and V_{SS} and high leakage current will flow. The second consideration is to minimize the test set. We define a minimal complete leakage test set (MCLTS) for a CMOS circuit as a minimal set of tests capable of generating the maximum possible information about transistor leakage conductances, i.e., capable of generating the largest set of independent equations containing conductances.

For very simple structures MCLTS can be generated in a simple way. Consider, for example, individual inverter, NAND and NOR gates. The transistor level diagram of these gates and their corresponding MCLTSs are given in Fig. 6.1. The stuck-at faults tested by the same tests are also included for comparison.

For individual complex cells, an algorithmic way to generate MCLTs is possible. A graph-theoretic method is presented here. Let us consider the electrical lines, the nodes in a graph, and let the transistors be the edges. A cut-set is a set of transistors, removal of which will divide the graph into two separate parts. For example, in Fig. 6.2 {AP,CP} and {CN,DN,EN} are two of the cut-sets. A set of

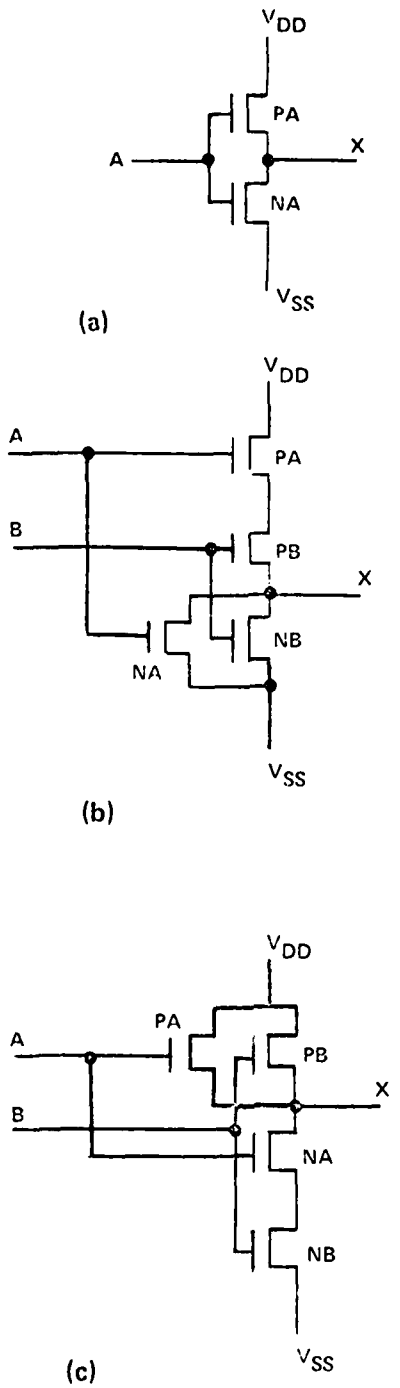

Fig. 6.1: Examination of (a) inverter; (b) NOR; (c) NAND gates.

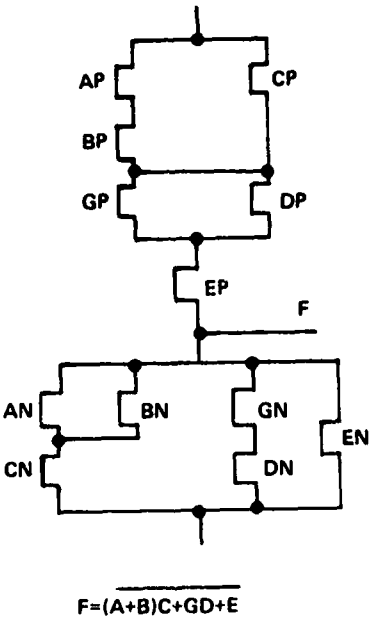

Fig. 6.2: A complex cell.

independent cut-set generates independent equations. We will view the graphs as consisting of several subgraphs, called serial groups, all connected in series. In Fig. 6.3, there are four serial groups, consisting of the {AP,BP,CP}, {GP,DP}, {EP} and {AN,BN,CN,GN,DN,EN}. The test generation method consists of the following steps:

1. Identify all serial groups.
2. For each serial group, find the largest set of linearly-independent cut-set.
3. Generate a test vector for each cut-set such that the transistors in the cut-set are OFF and are connected to both V_{DD} and V_{SS} through a low resistance path.

Example 2: For Fig. 6.2, the independent cut-sets are given below:

{AP,CP}, {BP,CP}

{GP,DP}

{EP}

{AN,BN,GN,EN}, {CN,GN,EN}, {CN,DN,EN}.

Consequently, a minimal CLTS is (in terms of A,B,C,D,E,G): 101000, 011000, 000101, 000010, 001100, 110100, 110001.

An important result for complex cells (NAND and NOR gates are special cases of it) is given below:

Theorem 1: For any individual complex cell, a MCLTS consists of n/2+1 tests, where n is the number of transistors.

Proof: Consider first the structure of complex cells. Starting from an inverter, any complex cell can be formed by a number of modification steps. In each step, two transistors (one P-type, other N-type) are added, one in parallel with a set of transistors (or a single

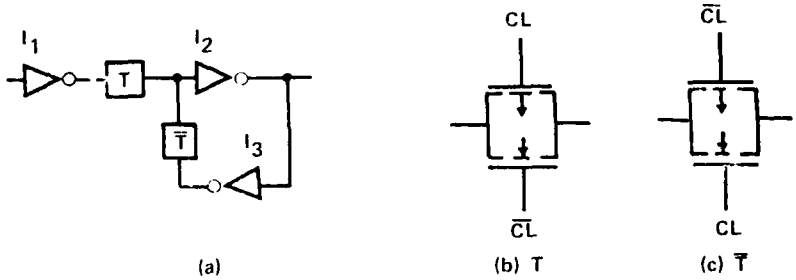

Fig. 6.3: A common transmission-gate structure.

transistor), and the other in series with the complimentary set of transistors in the complementary part. For a complex cell with n transistors (n-2)/2 such steps are needed.

Each modification step adds only one additional independent cut-set. The transistor which is added in parallel to a set S of transistors, simply has to be added to all indpendent cut-sets of S. The transistor which is added in series to the complementary set of transistors S' will require an additional cut-set.

An inverter requires two cut-sets. The rest of n-2 transistors will add (n-2)/2 cut-sets. Thus the maximal number of independent cut-sets as well as the number of tests required is $2+(n-2)/2 = n/2+1$ □

A MCLTS for a circuit consisting of a number of gates, complex cells, etc. will contain a MCLTS for each element. For such circuits, MCLTS can be obtained by considering all available test patterns, and then removing those which provide only redundant information. If an incomplete set of tests is available (for example, those generated for stuck-at testing), the set of undetected faults can be obtained by simulation. Additional tests for these undetected faults can be generated and added.

NAND, NOR and inverter-gates and complex cells provide a circuit that connects V_{DD} and V_{SS}. Conductances of these elements appear in parallel across V_{DD} - V_{SS} lines. The overall conductance is then simply the sum of conductances of all elements.

The transmission-gates can complicate the situation by creating cross-paths. A common transmission gate configuration is shown in Fig. 6.3. The transmission gate $T(\bar{T})$ presents a low resistance path

when CL=0(1) for either direction, otherwise, both transistors are OFF, and it presents a high resistance path. The voltage across $\bar{T}$ in Fig. 6.3a is always zero in a static situation, hence it will never contribute to overall conductance. The transistors in $\bar{T}$ cannot be tested for leakage faults. The leakage in the transistors in T can be tested if it is OFF, and outputs of I_1 and I_3 (since $\bar{T}$ is ON) are of opposite logical values. The conductance of transistors in T will appear across V_{DD} and V_{SS}, in parallel with other elements.

Relationship Between Logical Testing and Leakage Testing

It is important to consider the relationship between logical and leakage testing. Let us first consider only networks consisting of inverter, NAND and NOR gates.

Each gate consists of a set of serial elements (s.e.) which are transistors or a parallel combination of transistors. As no distinction can be made among a set of parallel transistors, they are regarded as a single s.e. Each s.e. allows a small leakage current when it is OFF.

Theorem 2: For an independent NOT, NOR or NAND gate, the minimum stuck-at fault test-set is the complete leakage test-set (test-set which enables the leakage current of each s.e. to be determined). From this set each test pattern tests one s.e. for leakage current as well as one stuck-at fault set containing at least one unique fault not tested by other vectors.

Proof: The proof is apparent when one considers the tables in Fig. 6.1. For example, A stuck-at-1 is only testable by AB=01 for the NAND gate.

Corollary 1: For a NOT, NOR or NAND gate, whenever the leakage current is determined by a single serial element, the corresponding stuck-at fault-set is tested and vice-versa.

Now let us consider a leakage test experiment. Each gate constitutes a parallel path for the total leakage current. For any jth vector the total measured leakage conductance includes the contribution from each gate:

$$\sum_i \text{(contribution from gate i under vector j)} = C_j.$$

Contribution from each gate would either be controlled by a single s.e. or by a series combination of s.e. For a gate, let the leakage conductance due to the kth s.e. or unique series combination of serial elements be denoted by C_k. Then a v by s matrix M, consisting of 1's and 0's can be written such that

$$M \cdot C_k = C_j \qquad (1)$$

where v is the number of input vectors and s is the total number of serial elements and unique series combinations of all gates. An element of M, $m_{kj} = 1$ whenever kth element contributes conductance when jth vector is applied, 0 otherwise, $k = 1,2,\ldots,s$ and $j = 1,2,\ldots,v$.

Example 1 shows the set of equations for $v = 4$, $s = 4$. The first equation contains a series combination of serial elements. The last equation deals with the contribution from a serial element consisting of PA and PB in parallel.

Eq. (1) is a system of linear equations in C_k's. Now we will show that for a minimal stuck-at fault test-set, the resulting system of

equations is linearly independent. We will do so by considering only those columns of M which correspond to a single s.e. If the rows of M are linearly independent when some of the columns are not considered, then they are also linearly independent with all the columns. Let us form a matrix M* which has only those columns of M which correspond to the s.e.'s of all gates. For instance, in Example 1, the M* contains columns corresponding to elements NA, NB, and the parallel combination of PA and PB.

Theorem 3: If M* is obtained for a minimal stuck-at fault test-set, then all its rows are linearly independent.

Proof: Consider a vector p (corresponding to a row), it must test at least one stuck-at fault f_1 which is not tested by any other. The fault f_1 corresponds to the leakage conductance controlled by a specific s.e., and hence the corresponding row of M* has a 1 in the corresponding place. No other row can have a 1 in this column, because it would mean that another test-vector, say q, would cause contribution of this s.e. to its total leakage conductance, which in turn would mean that q also tests f_1.

Since each row of M* has a 1 in a column, where no other row has a 1, all the rows are linearly independent.

If a stuck-at test set is available which is minimal and complete, then by Theorem 3, all equations generated will be linearly independent, and by Corollary 1, all s.e. will be tested (i.e., their conductance will appear in the total conductance measured). This leads us to the following important result:

Theorem 4: For a network consisting of only inverter, NAND and NOR gates, a minimal complete stuck-at test-set will generate a set of equations in which (i) all equations are linearly independent and (ii) each variable will appear at least once.

This suggests that for such networks, a minimal stuck-at test-set can be used as a starting point for generating a MCLTS. This also indicates that leakage testing and logical testing based on stuck-at fault-model can be done at the same time since a large fraction of vectors are good for both.

Correspondence between logical and leakage testing is even better if stuck-open and stuck-on fault model is used, which is perhaps more appropriate for MOS and SMOS because:

--A logical test, which tests for a stuck-open transistor, will turn its complimentary transistor OFF, with *about* $V_{DD} - V_{SS}$ potential across it. It is, therefore, a leakage test for the complimentary transistor.

--The stuck-on faults are not always testable by logical testing. In order to excite a stuck-ON transistor, a vector is necessary to turn the transistor-under-test OFF, and to connect its terminals to V_{DD} and V_{SS} through low resistance paths. If the transistor is indeed stuck-ON, the output of the gate or complex cell containing this transistor will be connected to both V_{DD} and V_{SS} through low resistance path. The logical output can then be either the same as or different from the normal output depending on the resistance involved. Generally, stuck-ON faults in the load part cannot be detected by logical testing (6.1).

Leakage testing is very effective in this case. Any stuck-ON fault will be automatically tested when the complimentary transistor is tested for stuck-open faults.

Therefore, leakage testing can be effectively and naturally combined with logical testing for stuck-open faults.

REFERENCES

[6.1] A.K. Bose, et al., "A Fault Simulator for MOS LSI Circuits," Proc. 19th Design Automation Conference, June 1982, pp. 400-409.

VII. ANALYSIS OF EXPERIMENTAL DATA: METHODS

In order to evaluate the effectiveness of leakage testing, a probabilistic analysis of the problem is required. This requires analysis of experimental data. Some data is available from "Digital Microcircuit Characterization and Specification" [7.1]. It includes device description and supply current data for five CMOS devices. Several samples of each device were examined for logical integrity and leakage current under different vectors. All had logically correct performance but the leakage current was excessive in some cases. We analyzed the data to seek the following information:

1. Identify possible leaky transistors.
2. Calculate the average normal leakage conductance and its variance.
3. Find the distribution of abnormal leakage conductance.

The average normal conductance per transistor for a chip can be determined by using either Procedure A or Procedure B given below. It is assumed that all normal transistors within a chip have about equal conductance, as is suggested by the experimental data. Some transistors may have dimensions different from the rest; their conductance will be different from others. This fact can be taken into account if desired, but can be ignored without significantly affecting the accuracy. For simplicity, the effect of protection diodes is also ignored here.

Procedure A

1. Assume each transistor has unit conductance of G ohm^{-1}.
2. For any specific input vector V_i, the transistor level diagram can be used to compute the total conductance. Let it be equal to N_iG where N_i is not ncessarily an integer.
3. For this same vector V_i, let the measured conductance be C_i. Then for V_i the average conductance per transistor is given by

$$G = C_i/N_i.$$

4. Steps 2 and 3 are repeated for all vectors, and the resulting values are averaged.

The disadvantage of Procedure A is that a lot of work is required because the entire circuit has to be analyzed for each input vector. An approximate procedure can be found which requires significantly less work because only one element of each kind has to be analyzed for all input vectors of that element. This, called Procedure B here, is based on the following observations:

1. Experimental data shows that the total normal conductance is about equal for all vectors [7.1].
2. The transistor level diagrams for several circuits such as BCD-to-Decimal decoder, a section of ALU, were analyzed for all input vectors. For each circuit, assuming all transistors have equal conductance, the total conductance was found to be about equal for all vectors.

We can, therefore, reasonably assume that in general, for devices with more than just a few gates, all N_i are about equal. The assumption should be even better for larger devices, since the sample size is

greater, and the average should be closer to the expected value. Exceptions to this may be possible for devices with very regular structure and regular signal values. Such cases can be handled by Procedure A.

Procedure B

1. Identify basic elements such as gates, complex cells, etc. The total conductance of the device is equal to the sum of the conductances of the individual elements.
2. For each element, find conductances for all V_i and average them to find average conductance. This, of course, assumes that the occurrence of all vectors are equally likely.
3. The approximate average conductance for a chip is given by the sum of average conductance of all its elements. Let this be equal to MG, where M is a positive number, not necessarily an integer.
4. The average conductance per transistor is then given by

$$G = \frac{\text{average of measured conductances}}{M}.$$

Steps 1 and 2 can be carried out for a number of commonly used elements, and the results can be used to analyze any general circuits.

Inverter (Fig. 7.1): For an inverter only two input vectors, 0 and 1, are possible. The conductance in both cases is G, hence the average conductance is G.

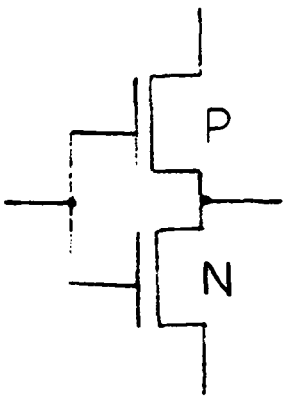

Fig. 7.1: Inverter.

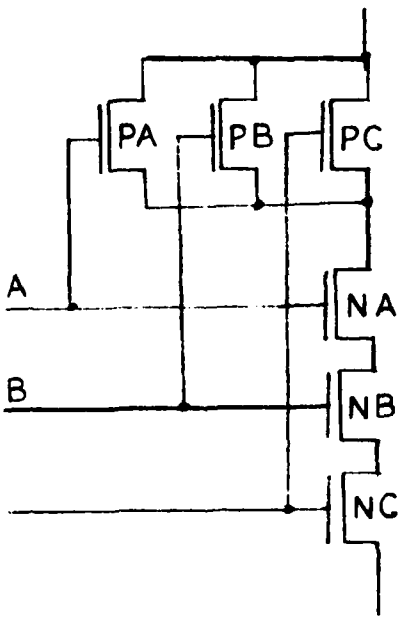

Fig. 7.2: 3-input NAND gate.

Input	Conductance Controlled by	Value in G	Average
0	N	1	1
1	P	1	

Table 7.1: Conductance for inverter.

Notice that the overall conductance value is controlled by a subset of the OFF transistors. The ON transistors will not show up in the total value.

NAND and NOR gates (Figs. 7.2 and 7.3): Let us first consider three input NAND and NOR gates (Tables 7.2 and 7.3). The results can be easily extended to NAND and NOR gates with any number of inputs.

Inputs A	B	C	Conductance Controlled by	Value in G	Average
0	0	0	S(NA,NB,NC)	1/3	0.979
0	0	1	S(NA,NB)	1/2	
0	1	0	S(NA,NC)	1/2	
0	1	1	NA	1	
1	0	0	S(NB,NC)	1/2	
1	0	1	NB	1	
1	1	0	NC	1	
1	1	1	P(PA,PB,PC)	3	

Table 7.2: Conductance for NAND gate.

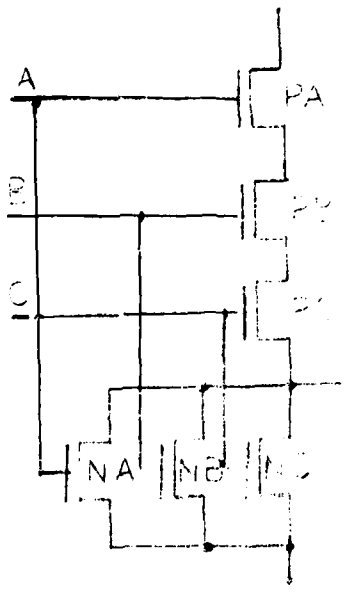

Fig. 7.3: 3-input NOR gate.

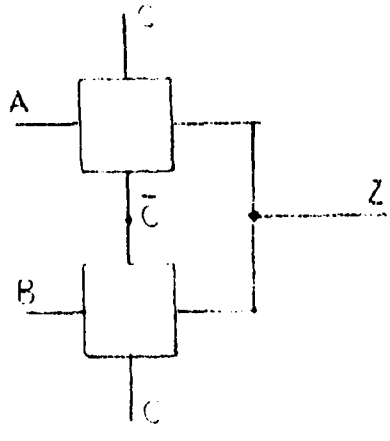

Fig. 7.4: Transmission-gate pair (type 1).

In the table, S(NA,NB,NC) and P(PA,PB,PC) etc. imply the serial or parallel combinations of the transistors in the parenthesis.

Inputs A	B	C	Conductance Controlled by	Value in G	Average
0	0	0	P(NA,NB,NC)	3	
0	0	1	PC	1	
0	1	0	PB	1	
0	1	1	S(PB,PC)	1/2	
1	0	0	PA	1	0.979
1	0	1	S(PA,PC)	1/2	
1	1	0	S(PA,PB)	1/1	
1	1	1	S(PA,PB,PC)	1/3	

Table 7.3: Conductance for NOR gate.

The average conductance for both NAND and NOR gates is the same. If all input vectors are equally likely, the average conductance for an n-input NAND and NOR gates can be computed. One input vector will turn all parallel transistors OFF, giving conductance equal to n·G. A vector that turns k series transistors OFF causes conductance of G/k. Of n series transistors, k can be chosen in $\binom{n}{k} = (n!)/(k!n-k!)$ ways. The average conductance then is

$$\frac{1}{2^n}\left\{n + \sum_{k=1}^{n} \frac{n!}{k!(n-k)!} \frac{1}{k}\right\}G.$$

For example, for 2, 3 and 4 input NAND or NOR gates the average conductance is 1.125 G, 0.979 G and 0.786 G, respectively.

Transmission gates: Transmission gates (TG) are generally used in pairs or in groups. Some common configurations are considered below.

In Fig. 7.4, the output Z can be chosen to be equal to either A or B. Let us assume that inputs A, B and C may independently assume any values. Remembering that an OFF transmission gate has both P-type and N-type transistors OFF, we can get Table 7.4.

Inputs A	B	C	Conductance Controlled by	Value in G	Average
0	0	0	-	0	
0	0	1	-	0	
0	1	0	P(PB,NB)	2	
0	1	1	P(PA,NA)	2	1
1	0	0	P(PB,NB)	2	
1	0	1	P(PA,NA)	2	
1	1	0	-	0	
1	1	1	-	0	

Table 7.4: Conductance for transmission gate pair in Fig. 7.4.

The second configuration is shown in Fig. 7.5. Here A or its complement $\bar{A}$ is selected. In Table 7.5, the conductance of the transmission gate pair only is given. In this, and in the following tables, conductances of the inverters are not included in the tables.

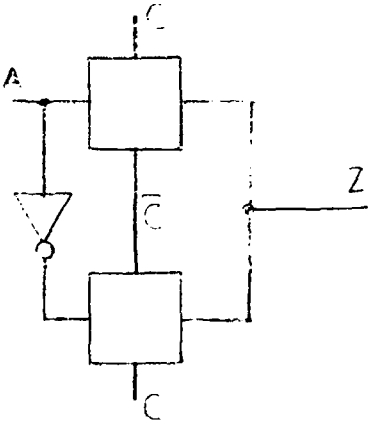

Fig. 7.5: Transmission-gate pair (type 2).

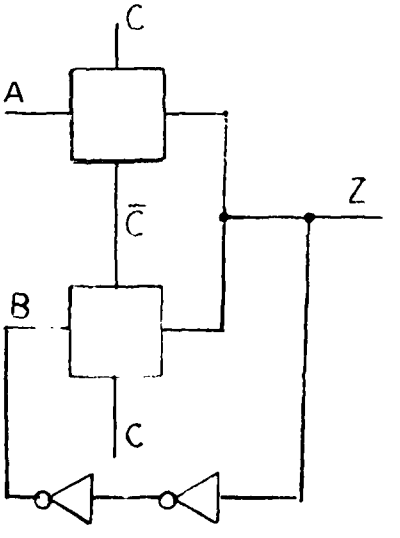

Fig. 7.6: Transmission-gate pair (type 3).

Inputs A	C	Conductance Controlled by	Value in G	Average
0	0	P(PB,NB)	2	
0	1	P(PA,NA)	2	
1	0	P(PB,NB)	2	2
1	1	P(PA,NA)	2	

Table 7.5. Conductance for transmission gate pair in Fig. 7.5.

In Fig. 7.6, the output value Z is fed back through two inverters. The loop serves as storage element. When TG A is ON and TG B is OFF, there is no leakage current as voltage across TG is zero. When TG A is OFF and TG B is ON, there will be a conductance of P(PA,NA) = 2 G, whenever the input A differs in value from the value in the storage loop.

Inputs A	B	C	Conductance Controlled by	Value in G	Average
0	0	0	-	0	
0	0	1	-	0	
0	1	0	not possible	-	
0	1	1	P(PA,NA)	2	
1	0	0	not possible	-	0.66
1	0	1	P(PA,NA)	2	
1	1	0	-	0	
1	1	1	-	0	

Table 7.6: Conductance for transmission gate pair in Fig. 7.6.

A more complicated situation is shown in Fig. 7.7. The feedback loop contains a controlling element (a NOR gate in this case) with a controlling input. Notice that the total number of inversions within the loop is even, as is required for operation as a storage element. The TG B affects the total conductance when the controlling input breaks the loop and opposite logic values on the two terminals of the TG B are hence possible.

Inputs A	B	C	D	Controlled by	in G	Average
0	0	0	0	-	0	
0	0	0	1	-	0	
0	0	1	0	-	0	
0	0	1	1	-	0	
0	1	0	0	not possible	-	
0	1	0	1	not possible	-	
0	1	1	0	P(PA,NA)	2	
0	1	1	1	not possible	-	
1	0	0	0	not possible	-	0.8
1	0	0	1	P(PB,NB)	2	
1	0	1	0	P(PA,NA)	2	
1	0	1	1	P(PA,NA)	2	
1	1	0	0	-	0	
1	1	0	1	not possible	-	
1	1	1	0	-	0	
1	1	1	1	not possible	-	

Table 7.7: Conductance for transmission gate pair in Fig. 7.7.

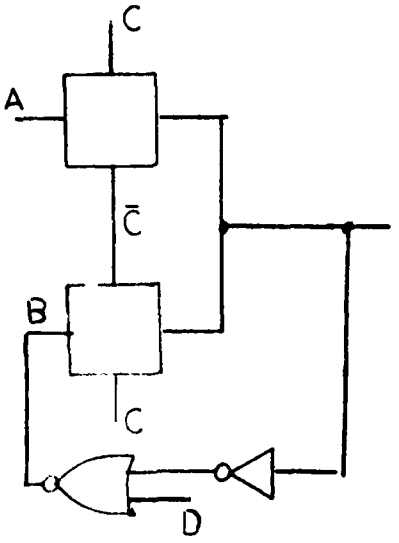

Fig. 7.7: Transmission-gate pair (type 4).

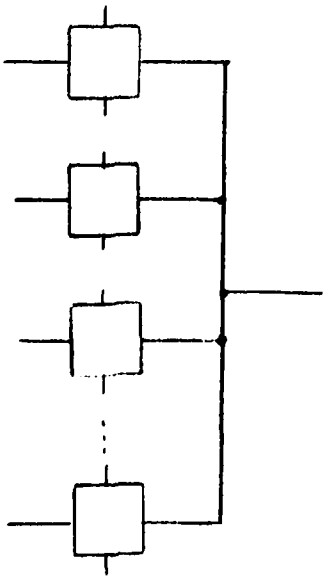

Fig. 7.8: Group of transmission-gates.

Fig. 7.8 shows n TGs used in a group. At any given time only one TG is ON, and the other (n-1) are CFF. For any OFF TG, the probability that the logical values across it are different is 1/2. As an OFF TG with different logical values across it contributes 2 G to the total conductance, the average conductance for the structure is $(1/2)(n-1)\cdot 2\ G = (n-1)G$. This assumes that each TG has 1/n probability of being on. However, if it is allowed that all transmission gates may be OFF (i.e., if the boolean expression C1 + C2 + ... + Cn is not identically 1), then the average conductance is

$$\frac{n}{n+1}(n-1) + \frac{1}{(n+1)} \cdot n = \frac{n^2}{n+1}\ G.$$

In other situations, when several transmission gates are used in a cluster, each situation will require individual analysis.

Complex cells: As different complex cells have different structures, each has to be analyzed separately. Let us consider the complex cell shown in Fig. 7.9. The corresponding conductances are computed as shown in Table 7.8.

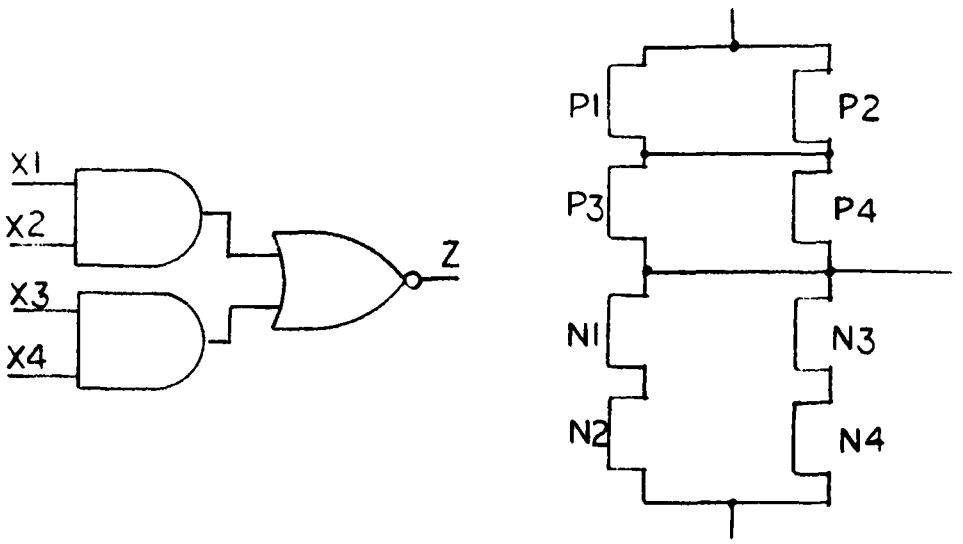

Fig. 7.9: A complex cell.

Inputs X1	X2	X3	X4	Conductance Controlled by	Value in G	Average
0	0	0	0	P(S(N1,N2),S(N3,N4))	1	
0	0	0	1	P(S(N1,N2),N3))	1.5	
0	0	1	0	P(S(N1,N2),N4))	1.5	
0	0	1	1	P(P3,P4)	2	
0	1	0	0	P(N1,SCN3,N4))	1.5	
0	1	0	1	P(N1,N3)	2	
0	1	1	0	P(N2,N4)	2	
0	1	1	1	P(P3,P4)	2	
1	0	0	0	P(N2,S(N3,N4))	1.5	1.75
1	0	0	1	P(N2,N3)	2	
1	0	1	0	P(N2,N4)	2	
1	0	1	1	P(P3,P4)	2	
1	1	0	0	P(P1,P2)	2	
1	1	1	0	P(P1,P2)	2	
1	1	1	0	P(P1,P2)	2	
1	1	1	1	S(CP(P1,P2),P(P3,P4))	1	

Table 7.8: Conductance for complex cell of Fig. 7.9.

Other structures: Sometimes inverters with connected-AND and connected-OR structures are used, as shown in Figs. 7.10 and 7.11. They require fewer transistors then would otherwise be required. The corresponding conductances for connected-AND and connected-OR are given in Tables 7.9 and 7.10 respectively.

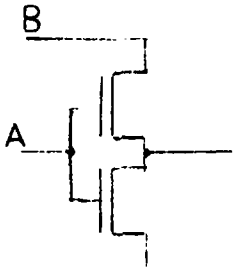

Fig. 7.10: Connected-AND.

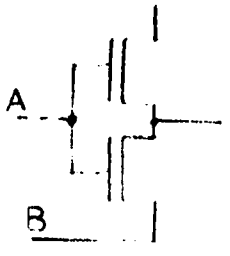

Fig. 7.11: Connected-OR.

Inputs A	Inputs B	Conductance Controlled by	Value in G	Average
0	0	-	0	0.5
0	1	NA	1	
1	0	-	0	
1	1	PA	1	

Table 7.9: Conductance for connected-AND (Fig. 7.10).

Inputs A	Inputs B	Conductance Controlled by	Value in G	Average
0	0	NA	1	0.5
0	1	-	0	
1	0	PA	1	
1	1	-	0	

Table 7.10: Conductance for connected-OR (Fig. 7.11).

REFERENCES

[7.1] M. Ostrowski, "Digital Microcircuit Characterization and Specification," General Electric Company Report for Rome Air Development Center, August 1975.

VIII. ANALYSIS OF EXPERIMENTAL DATA: RESULTS

The available data is for five devices [8.1]. Few chips of each type were examined. All had logically correct performance, but some exhibited excessive leakage. The GE report [8.1] assumes leakage to be excessive when the supply current exceeds 500 nA. However, by a cursory examination of the data, it appears that 100 nA may be a more natural limit for these devices. This view is supported by the processed results.

In the following analysis some simplifying assumptions are made:

1. All devices use the same technology and approximately the same transistor dimensions.
2. Protaction-diodes have been ignored for simplicity. It is not clear how much conductance they contribute. As all devices considered here have a large number of gates, this assumption should not significantly affect the accuracy.
3. Only a few transistors are more likely to be bad than a large number of transistors. When some (but not all) vectors cause excessive leakage of approximately the same value, it is probably from the same equivalent leakage fault-set. It is assumed that only one particular transistor in the equivalent leakage fault-set is leaky.
4. For some of the devices, the report [8.1] gives only gate-level diagrams. As for them the transistor-level diagram

were not obtainable, it has been assumed that the gate-level diagrams directly represent transistor-level diagrams.

A note is required here to explain the computation of conductance. The devices are divided into components, which were individually examined in the previous section. The total conductance is the sum of contributions of individual components. The method is based on this observation. If an OFF transistor (or a group of transistors) connect the two nodes which have the opposite logical values 0 and 1, then the transistor (or the group) is essentially connected between V_{DD} and V_{SS}, through low resistance connections. Its conductance, thus, can be added directly to the rest of the total conductance to obtain the total conductance.

The analysis for the five devices is presented below.

A: CD4028A BCD-to-Decimal Decoder

Fig. 8.1 gives a gate-level diagram for the device. Table 8.1 gives a set of vectors, which were applied to five different chips and the corresponding leakage current values measured.

It is instructive to compare the average conductance values used for Procedures A and B. By examination of individual vectors and the transistor-level diagram, values in Table 8.2 were obtained.

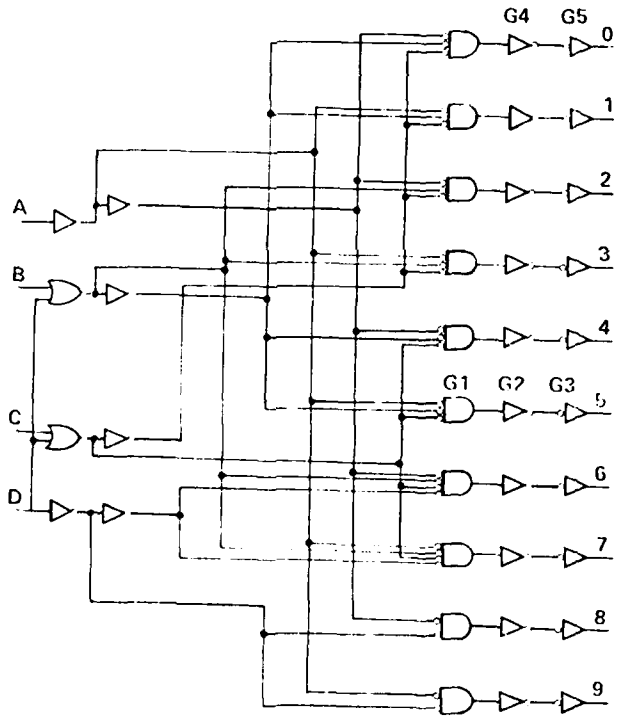

Fig. 8.1: BCD to decimal decoder.

INPUT VECTOR				OUTPUTS										CHIPS				
D	C	B	A	"0"	"1"	"2"	"3"	"4"	"5"	"6"	"7"	"8"	"9"	#1	#2	#3	#4	#5
0	0	0	0	1	0	0	0	0	0	0	0	0	0	1.8×10^{-1}	4.7	1.13	4.4×10^{-1}	2.0×10^{-1}
0	0	0	1	0	1	0	0	0	0	0	0	0	0	1.8×10^{-1}	5.1	1.75×10^{5}	4.6×10^{-1}	2.0×10^{-1}
0	0	1	0	0	0	1	0	0	0	0	0	0	0	1.8×10^{-1}	4.5	1.75×10^{5}	4.2×10^{-1}	1.9×10^{-1}
0	0	1	1	0	0	0	1	0	0	0	0	0	0	1.8×10^{-1}	4.8	1.75×10^{5}	4.5×10^{-1}	2.1×10^{-1}
0	1	0	0	0	0	0	0	1	0	0	0	0	0	1.8×10^{-1}	4.9	1.75×10^{5}	4.5×10^{-1}	2.1×10^{-1}
0	1	0	1	0	0	0	0	0	1	0	0	0	0	1.9×10^{-1}	5.8	1.75×10^{5}	2.9×10^{5}	2.2×10^{-1}
0	1	1	0	0	0	0	0	0	0	1	0	0	0	1.8×10^{-1}	5.0	1.7×10^{5}	4.6×10^{-1}	2.0×10^{-1}
0	1	1	1	0	0	0	0	0	0	0	1	0	0	1.95×10^{-1}	6.0	1.7×10^{5}	5.5×10^{-1}	2.1×10^{-1}
1	0	0	0	0	0	0	0	0	0	0	0	1	0	1.7×10^{-1}	4.4	1.7×10^{5}	4.5×10^{-1}	2.0×10^{-1}
1	0	0	1	0	0	0	0	0	0	0	0	0	1	1.8×10^{-1}	4.8	1.7×10^{5}	4.8×10^{-1}	2.0×10^{-1}

Table 8.1: Experimental data (in nanoamperes) for CD4028A chips.

Input Vector D	C	B	A	Total Conductance in G	Average
0	0	0	0	39.3	
0	0	0	1	38.3	
0	0	1	0	35.3	
0	0	1	1	38.8	
0	1	0	0	37.8	37.7
0	1	0	1	38.8	
0	1	1	0	38.8	
0	1	1	1	38.8	
1	0	0	0	36.3	
1	0	0	1	36.3	

Table 8.2: Conductance values for CD4028A.

Using Procedure B, we have

26 inverters	26 x 1
4 2-input gates	4 x 1.125
6 3-input gates	6 x 0.979
2 4-input gates	2 x 0.786
38 gates	M = 37.94

The approximate value 37.94 is quite close to the individually computed values of 36.3 to 39.3 with average 37.7.

It can be seen by inspection of Table 8.1 that the chips 1, 2 and 5 show only normal leakage currents. Chip 3 shows normal leakage of 1.13 nA and abnormal leakage of about 1.73×10^5 nA. Since the abnormal

leakage values are about the same (allowing for limited measuring accuracy), it is likely that they are caused by a single transistor. Chip 4 shows normal leakage of about 0.462 nA (average) and abnormal leakage of 2.9×10^{5}. The normal per transistor conductance can be obtained by dividing the average normal leakage current by 15 volts x 37.94. As the abnormal leakage current is assumed caused by a single transistor for chips 3 and 4, the abnormal transistor conductances for them are obtained by dividing the abnormal leakage current values by 15 volts. The results are shown in Table 8.3.

	Chip 1	2	3	4	5
Normal Conductance Per Transistor	3.19×10^{-13}	8.78×10^{-12}	1.98×10^{-12}	8.12×10^{-13}	3.58×10^{-13}
Abnormal Transistor Conductances	-	-	1.15×10^{-5}	1.93×10^{-5}	-

Table 8.3: Conductances for CD4028A in ohm^{-1}.

For both chips 3 and 4, it is possible to identify a small set of transistors which includes the leaky transistor. For chip 3, it can be seen that excessive leakage of about 1.7×10^{5} nA occurs whenever output line 0 is logically 0. When output line 0 is logically 1, excessive leakage does not occur. Assuming that a few transistors are more likely to be faulty than a large number, we can suspect that there is leaky transistor in the three gates associated with the output 0. As the faulty transistor is sensitized, when the output 0 is logically 0,

the leaky transistor is sensitized (i.e., normally OFF) when input vector 0000 is applied. The suspected transistor set (STS), then, can be narrowed down to {N-type in inverter G4, P-type in inverter G5}. The NOR gate in series with G4 and G5 would produce the effect only if all three series transistors are leaky. The faults in the STS are equivalent, no distinction can be made between them.

Similarly for chip 4, the STS is {N-type transistors in NOR G1, P-type in inverter G2, N-type in inverter G3}.

B: CD4029A Presettable Up/Down Counter

Fig. 8.2 gives a gate-level diagram for the device. The transistor-level diagram for the flip-flops was available (Fig. 8.3). For the rest of the device, transistor-level diagram was not available, and was constructed from the gate-level description. It was assumed that CMOS structures: inverters, NAND and NOR gates, complex cells and connected-AND and OR gates were used so that fewest number of transistors were required.

Using Procedure B, we can find the approximate average conductance.

For each of 4 flip-flops:

5 inverters	5 x 1 (in G)
1 TGP, type 2	2
1 TGP, type 3	0.66
2 TGP, type 4	0.8 x 2
13 gates	9.26

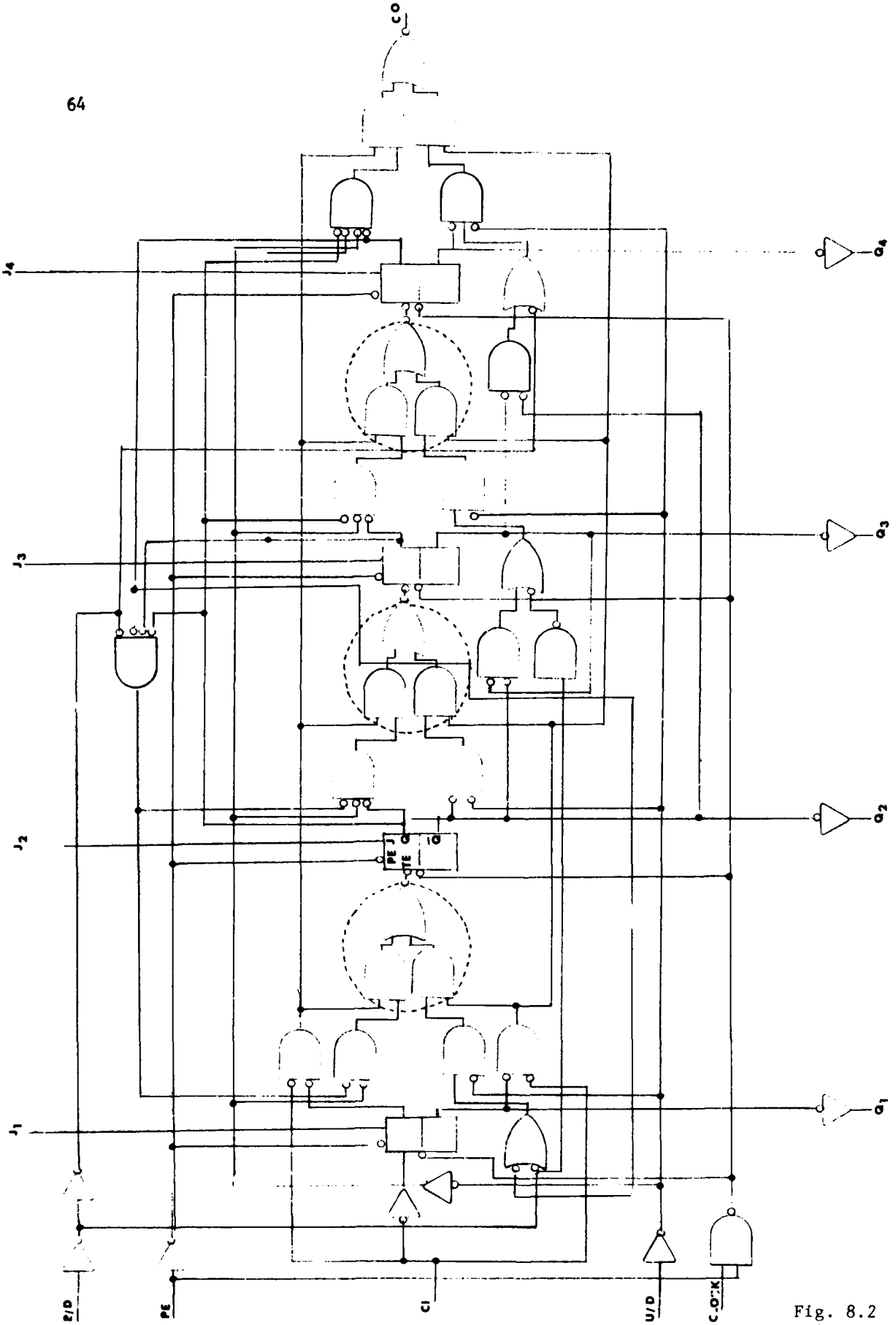

Fig. 8.2
CD4029A

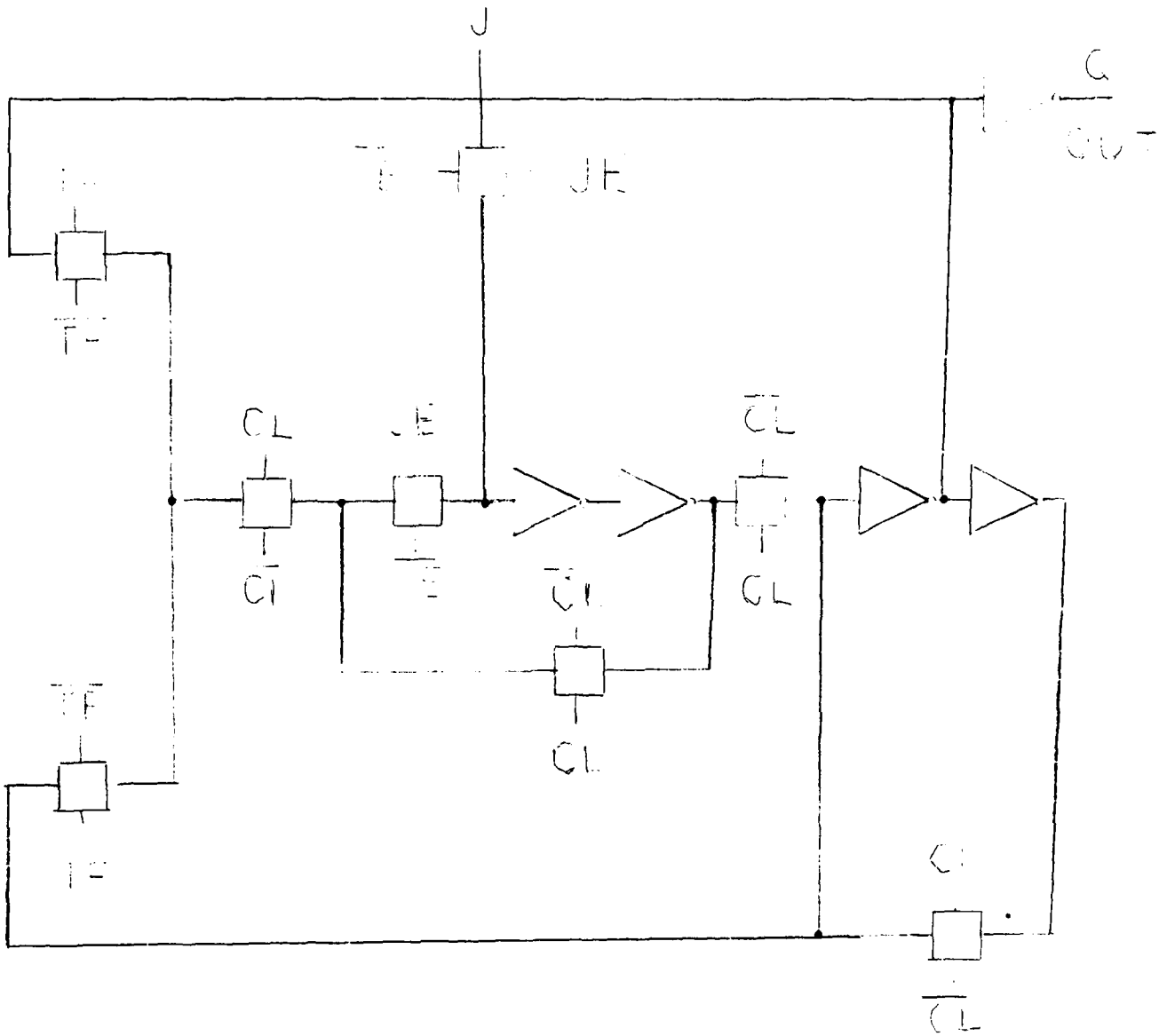

Fig. 8-3: Flip-flops in CD4029A.

Common circuitry:	
10 inverters	10 x 1
4 complex cells	4 x 1.75
6 connected gates	6 x 0.5
8 2-input gates	8 x 1.125
2 3-input gates	2 x 0.979
2 4-input gates	2 x 0.786
32 gates	32.53
Total:	
Common circuitry (32 gates)	32.53
Four flip-flops (52 gates)	37.04
84 gates	69.57 = M

Table 8.4 gives a set of vectors and corresponding leakage current values for five chips that were examined. It is seen that several ranges of values are obtained. The mean and standard deviation for these ranges are listed in Table 8.5

INPUTS									OUTPUTS					CHIPS				
PE	C1	B/D	U/D	CL	J_1	J_2	J_3	J_4	Q_1	Q_2	Q_3	Q_4	CO	#1	#2	#3	#4	#5
1	0	0	1	0	0	0	0	0	0	0	0	0	1	384	4. 3	208	133	1.37
1	0	0	1	0	1	0	1	0	1	0	1	0	1	366	4.66	153	134	2.06
1	0	0	1	0	0	0	1	1	0	0	1	1	1	382	4.69	210	133	1.56
1	0	0	0	0	0	0	0	1	0	0	0	1	1	383	4.71	209	134	1.41
1	1	0	0	0	1	0	1	0	1	0	1	0	1	385	4.70	153	133	1.43
1	0	0	0	0	0	1	0	0	0	1	0	0	1	383	25.1	209	133	1.37
1	1	0	0	0	0	0	0	0	0	0	0	0	1	382	0.703	207	133	1.87
1	0	1	1	0	0	1	0	1	0	1	0	1	1	1.5×10^4	21.0	1.8×10^3	961	1.60
1	0	1	1	0	0	1	1	1	0	1	1	1	1	1.52×10^4	12.6	1.8×10^3	961	1.70
0	0	1	1	0	1	1	1	1	1	1	1	1	0	1.52×10^4	10.8	1.8×10^3	828	2.16
1	0	1	0	0	1	0	0	0	1	0	0	0	1	1.58×10^4	0.75	233	134	1.96
0	0	1	0	1	1	0	0	0	0	0	0	0	0	1.58×10^4	0.72	289	0.684	1.30

Table 8.4: Experimental data (in nanoamperes) for CD4029A.

	Chip 1	2	3	4	5
Normal	-	7.98,8	-	0.684,0	1.65,0.29
Abnormal	380,6.58	-	207.9,40.68	133.37,0.52	-
Abnormal	1.54×10^{4},0.037	-	1.8×10^{3},0	828,0	-

Table 8.5: Leakage current ranges for CD4029A.

The top row represents normal leakage (according to our presumption). The large standard deviation for chip 2 indicates that some transistors have slightly large (but still normal) leakage compared to others. The values for chip 4 require some explanation. There are four sets of values, about 133, 961, 828 and 0.684 nanoamperes. The value 0.684 does not involve any leaky transistors. The values of about 133 and 828 nA appear to be caused by two different transistors. The values of 961 (133+828) nA is obviously caused by sensitization of both leaky transistors. The most reasonable assumption is that there are two leaky transistors in chip 4. The normal per transistor conductance and the normal transistor conductances are listed in Table 8.6.

	Chip 1	2	3	4	5
Normal Conductance Per Transistor	-	7.64×10^{-12}	-	6.55×10^{-3}	1.58×10^{-12}
Abnormal Transistor Conductances	2.53×10^{-8}	-	1.38×10^{-8}	8.89×10^{-9}	-
	1.02×10^{-6}	-	1.2×10^{-7}	5.52×10^{-8}	-

Table 8.6. Conductances for CD4029A in ohm^{-1}.

Some suspected fault sets can be identified. For chip 1, the supply current of about 1.5×10^{4} correlates with B/D=1. The suspected fault set is {P-type in inverter G1, N-type in inverter G2 and the appropriate N-types in NAND gates G3 and G4}.

C. CD4034A of Stage Bi-directional Paralled1/Serial Input/Output Bus Register

Fig. 8.4 and Fig. 8.5 show the gate-level diagram of the device. Fig. 8.4 was obtained by using a transistor-level diagram which was available.

The approximate average conductance can be calculated as follows.

Common:	
10 inverters	10 x 1
4 2-input gates	4 x 1.125
1 3-input gates	1 x 0.979
1 complex cell	1 x 1.44
16 gates	16.92 G
One of eight stages:	
1-of-3 TG group	1 x 2
1-of-2 TG group	1 x 1.33 (both may be off)
2 TGP, type 3	2 x 0.66
15 inverters	1 x 15
24 gates	19.66 G

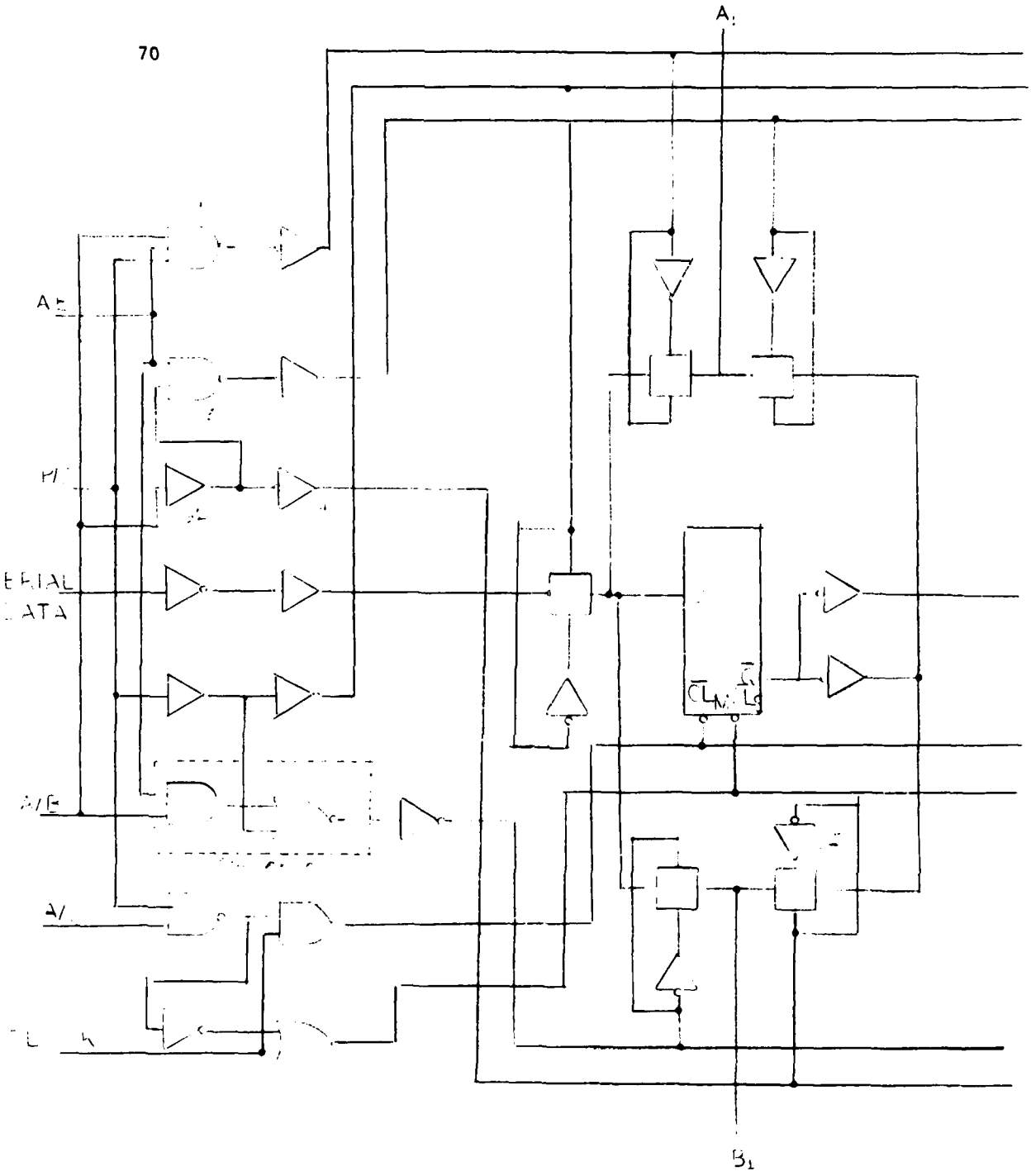

Fig. 8.4: CD4034A.

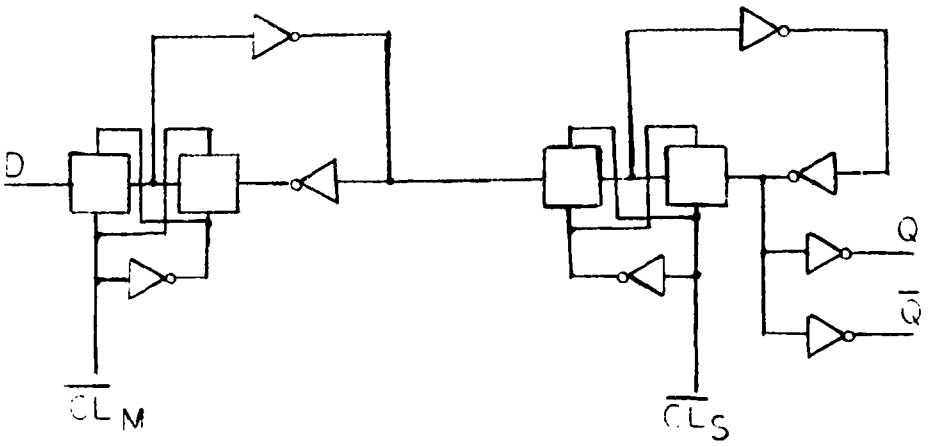

Fig. 8.5: A flip-flop in CD4034A.

Total:		
Common	(16 gates)	16.92
8 stages	(192 gates)	57.28
	208 gates	174.20 = M

Table 8.7 shows the leakage current values for the four chips tested. The average normal and abnormal supply current values are shown in Table 8.8.

INPUTS						INPUT/OUTPUT																CHIPS			
A/E	SD	A/B	P/S	A/S	CLK	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	#1	#2	#3	#4
1	1	1	1	1	0	0	1	0	1	0	1	0	1	-	-	-	-	-	-	-	-	2000	90	2.8	5.8
1	0	1	1	1	1	1	0	1	0	1	0	1	0	-	-	-	-	-	-	-	-	2000	63	8.4×10^5	6.2
1	0	1	0	0	1	1	0	1	0	1	0	1	0	-	-	-	-	-	-	-	-	2000	50	340	5.1
1	0	1	0	1	0	0	1	0	1	0	1	1	1	-	-	-	-	-	-	-	-	2000	25	320	5.8
0	0	1	1	0	0	0	1	0	1	0	1	1	1	-	-	-	-	-	-	-	-	1950	24	300	5.4
0	0	0	0	0	0	0	1	0	1	0	1	0	1	-	-	-	-	-	-	-	-	3.3	13	300	3.4
1	0	0	0	0	0	-	-	-	-	-	-	-	-	0	1	0	1	0	1	0	1	4.1	22	2.6	4.4
1	0	0	1	0	0	-	-	-	-	-	-	-	-	0	1	0	1	0	1	0	1	4.0	23	2.6	4.2

Table 8.7: Experimental data (in nanoamperes) for CD4034A.

	Chip 1	2	3	4
Normal	3.8, 0.44	32.5,16.91	2.66,0.14	5.04,0.56
Abnormal	1990,22.36	-	315,19.15	-
Abnormal	-	-	8.9×10^{5}	-

Table 8.8: Leakage current ranges for CD4034A.

The normal and abnormal transistor conductances are listed in Table 8.9.

	Chip 1	2	3	4
Normal Conductance Per Transistor	1.45×10^{-12}	1.24×10^{-11}	1.02×10^{-12}	1.93×10^{-12}
Abnormal Transistor Conductances	1.33×10^{-7}	-	2.1×10^{-8}	-
	-	-	5.8×10^{-5}	-

Table 8.9: Conductances for CD4034A chip.

For chip 1, the values of about 1990 nA are correlated with A/B=1. The suspected fault-set consists of these {PA/B in the complex cell, PA/B in the NAND G1, P in inverter G2, N2 in NAND G3, N in inverter G4, P in inverter G5}.

For chip 3, the causes of 8.4×10^{-5} and about 320 nA leakage are not readily identifiable, as the set of vectors is incomplete.

D. CD4090A 12-Stage Ripple Carry Binary Counter

The gate-level diagrams for this device are shown in Fig. 8.6. The transistor-level diagram was available. After consulting it, it was found that the inverter with ϕ input is actually what we have referred to as connected-OR.

The approximate average conductance is calculated below.

Common:

4 interters	4 x 1
2 2-input gates	2 x 1.125
1 inverter with connected-OR	1 x 0.5
7 gates	6.75 G

One of 12 stages:

3 inverters	3 x 1
2 2-input gates	2 x 1.125
2 TGP, type 4	2 x 0.8
9 gates	6.85 G

Total:

Common	(7 gates)	6.75
12 stages	(108 gates)	82.2
	115 gates	88.95 = M

For the five chips, the measure supply current values are listed in Table 8.10. Only four vectors were used. The normal and abnormal supply current ranges are given in Table 8.11.

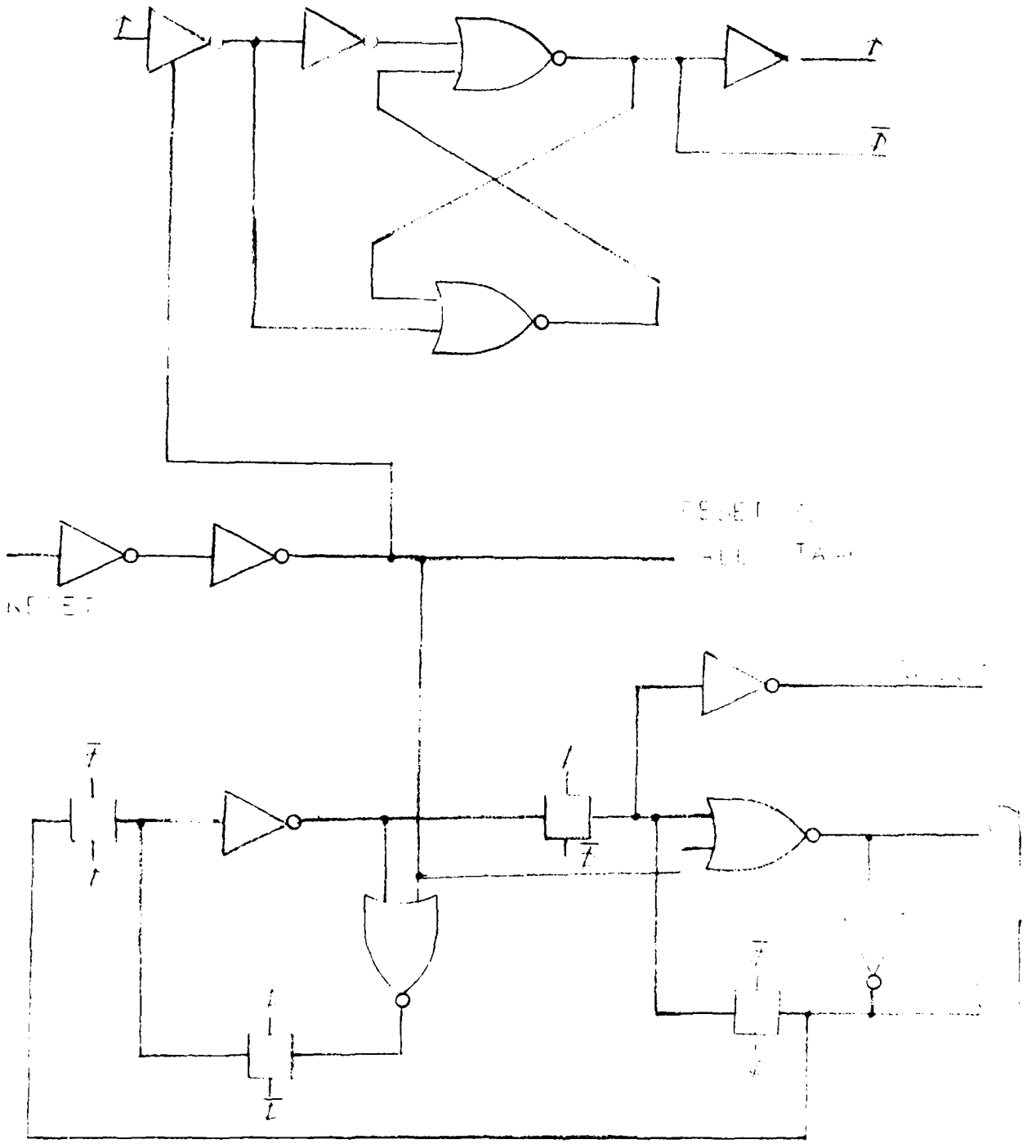

Fig. 8.6: CD4040A.

INPUTS		OUTPUTS												CHIPS				
RESET	INPUT	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9	Q_{10}	Q_{11}	Q_{12}	#1	#2	#3	#4	#5
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0.38	0.5	2.4×10^3	920	0.44
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.39	0.5	9.0×10^3	920	0.44
0	0	1	0	1	0	1	0	1	0	1	0	1	0	0.36	0.49	8.0×10^3	930	0.42
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0.36	0.50	7.4×10^3	920	0.41

Table 8.10: Experimental data (in nanoamperes) for CD4040A chip.

	Chip 1	2	3	4	5
Normal	0.3725,0.015	0.4975,0.005	-	-	0.4275,0.015
Abnormal	-	-	$2.4x10^3$,0	922.5,5	-
Abnormal	-	-	$8.13x10^3$,$8x10^2$	-	-

Table 8.11: Leakage current ranges for CD4090A.

The normal and abnormal transistor conductances are listed in Table 8.12.

	Chip 1	2	3	4	5
Normal Conductance Per Transistor	$1.8x10^{-13}$	$3.74x10^{-13}$	-	-	$3.18x10^{-13}$
Abnormal Transistor Conductances	-	-	$1.84x10^{-7}$	$1.63x10^{-6}$	-
	-	-	$4.8x10^{-7}$	-	-

Table 8.12: Conductance for CD4090A.

For chips 3 and 4, supply current is abnormal for all four vectors. Obviously, no suspected transistor set can be identified.

E. CD4042A Quadruple D Latch

Fig. 8.7 shows the gate-level diagram, which directly follows the transistor-level diagram.

The approximate average conductance is calculated as follows.

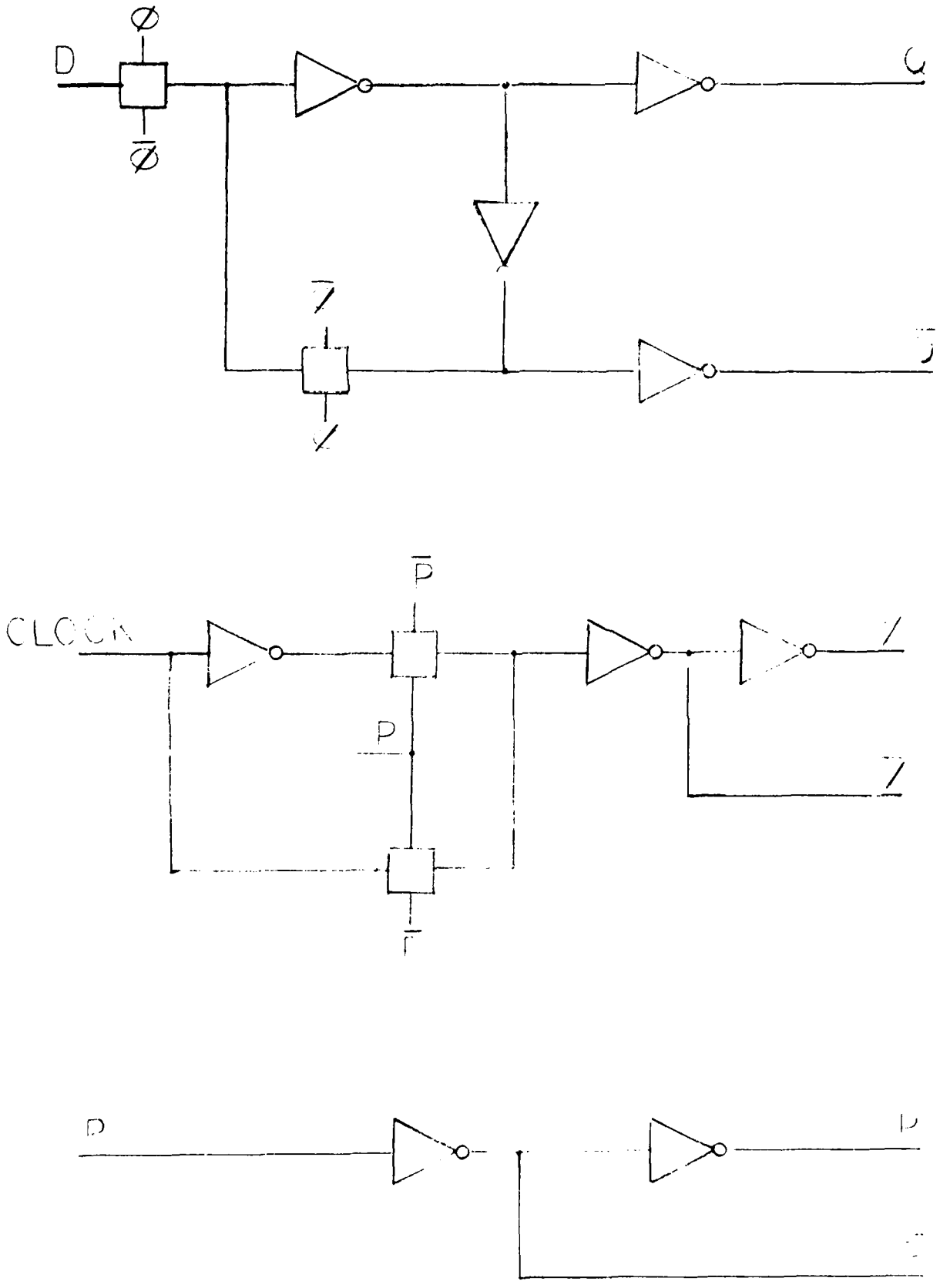

Fig. 8.7: CD4042A.

Common:	
5 inverters	5 x 1
1 TGP, type 2	1 x 2
7 gates	7 G
One of 4 latches:	
4 inverters	4 x 1
1 TGP, type 3	1 x 0.66
6 gates	4.66 G
Total:	
Common (7 gates)	7
4 Latches (24 gates)	18.64
31 gates	25.64 = M

For the three chips examined, the measured supply current values are given in Table 8.13. The normal and abnormal ranges of values are identified in Table 8.14.

INPUTS						OUTPUTS								DEVICES		
P	CL	D_1	D_2	D_3	D_4	Q_1	$\overline{Q}_1$	Q_2	$\overline{Q}_2$	Q_3	$\overline{Q}_3$	Q_4	$\overline{Q}_4$	#1	#2	#3
0	0	0	0	0	0	0	1	0	1	0	1	0	1	941	0.31	0.20
1	0	1	1	1	0	0	1	0	1	0	1	0	1	941	3000	0.18
1	1	1	1	1	1	1	0	1	0	1	0	1	0	0.49	0.31	0.18

Table 8.13: Experimental data (in nanoamperes) for CD4090A chip.

	Chip 1	2	3
Normal	0.49,0	0.31,0	$1.86\text{x}10^{-1}$,$1.15\text{x}10^{-2}$
Abnormal	941,0	3000,0	-

Table 8.14: Leakage current ranges for CD4042A.

The normal and abnormal transistor conductance values obtained are given in Table 8.15.

	Chip 1	2	3
Normal Conductance Per Transistor	$1.27\text{x}10^{-12}$	$8.06\text{x}10^{-13}$	$4.84\text{x}10^{-13}$
Abnormal Transistor Conductances	$6.27\text{x}10^{-8}$	$2\text{x}10^{-7}$	-

Table 8.15: Conductances for CD4042A.

As only three vectors were used, it is difficult to analyze the information. For chip 1, the values of 941 nA correlate with CL=0, as well as Q1=Q2=Q3=Q4=0. The suspected fault set is very large. For chip 2, the value of 3000 nA correlates with clock=0 and P=1. The suspected fault-set is {N in inverter G1, TG G2, P in inverter G3, N in inverter G4}.

Overall Results

Fig. 8.8 shows the distribution of conductances of normal and abnormal transistors on a logarithmic scale (with step-size of $\sqrt{10}$). The Y-axis for the normal per transistor conductance is the number of chips in (X, X $\sqrt{10}$) region of conductance. The Y-axis for the abnormal conductance is the number of transistors in (X, X $\sqrt{10}$) region of conductance. According to our computation, more than 4500 normal and 16 abnormal transistors are involved.

The normal part shows a sharp peak at about 10^{-12} ohm^{-1}. The abnormal part, also shows a peak at about 10^{-7} ohm^{-1}, but the distribution is quite flat. The gap between the two distributions (between 1.24×10^{-11} and 8.89×10^{-9}) is about three orders of magnitude wide. This gap is vital to the leakage current testing method.

It should be noticed that the normal conductance distribution is positioned between normal OFF conductance and normal ON conductance values. Devices which have any transistors with OFF conductance close to ON conductance (of about 10^{-1} ohm) would probably be screened out during conventional logical testing.

Looking at the data, it appears that the normal per transistor conductance within a chip is fairly constant, although we did not seek to obtain this distribution. This distribution would be quite difficult to obtain, and because of low variance (compared to other distributions), it is probably not necessary to seek this with accuracy.

Variation of normal per transistor conductance among the chips is significant. This is an expected result. Different chips, even though they may realize the same function, probably came from different

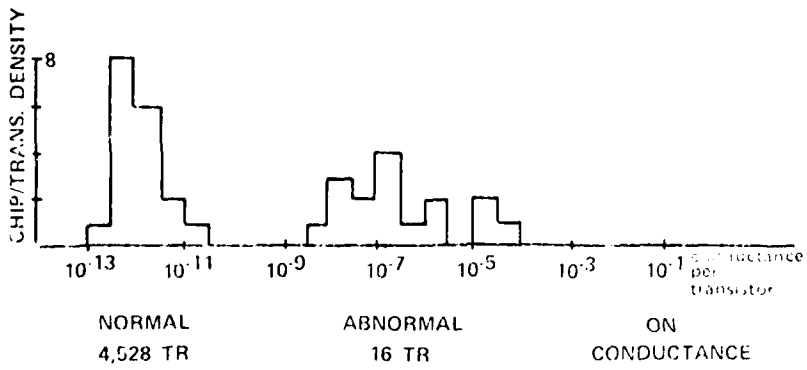

Fig. 8.8: Distributions for normal and abnormal conductances.

manufacturing batches, different wafers, or at least different areas of the wafer. Still, normal per transistor conductance varies within a narrower range as compared with the values of abnormal conductances.

Our analysis indicates that the total conductance (and hence the static supply current) is not correlated with the number of transistors in a direct way, as seen in Table 8.16 below. It seems to correlate better with the number of gates. We had counted each transmission-gate pair as two gates, if we count them as one, the correlation is even better. In that case, perhaps one G per gate may be a useful rule of thumb.

Device	Transistors	Gates(1)	Gates(2)	Conductance in G
4028	120	38	38	37.94
4029	228	84	68	69.57
4034	432	208	192	174.20
4040	232	115	91	88.95
4042	62	31	26	22.64

Gates(1), with TG pair counted as two, Gates(2) with TG pairs counted as one.

Table 8.16: Correlation of conductance with number of gates.

Probabilistic Analysis

A probabilistic analysis of the problem will be complex and some resonable assumptions would be required to keep the analysis tractable. These random variables are involved.

1. The normal leakage conductance within a chip: A glance at the experimental data suggests that the normal conductance of transistors within a chip varies very little. With the available data, it is not possible to obtain distribution of this random variable. However, as the distribution is very narrow, it can be assumed to be Gaussian, uniform or even point (with no variance) distribution. Considering the range of values involved (orders of magnitude) point distribution may be a good assumption.
2. Average normal leakage conductance among chips: The average normal leakage conductance has a very asymmetrical distribution, as shown in Fig. 8.8. Because of the asymmetry, a Weibull or Gamma distribution can be used.
3. Abnormal leakage conductance: This is also very asymmetrically distributed. The distribution is very wide compared to normal leakage conductance. A Weibull, Gamma or piecewise-linear distribution may be used.
4. Number of faulty transistors: For simplicity, we may assume a fixed, small probability of any transistor being leaky. Thus the probability of only a single transistor being leaky on a chip is significantly larger than the probability of a number of transistors being leaky. A bionominal distribution can be used.
5. Total normal chip conductance under an input-and-state vector: For a given vector, the total conductance is equal to the conductances contributed by each element (gate, complex cell,

transmission-gate etc.). The conductance contributed by an element can vary over a range of values. If the integrated circuit is large, then by the law of large numbers, the distribution of total normal conductance under a vector is approximately normal or Gaussian.

The experimental data clearly indicates that the total conductance values under different vectors are about equal, i.e. σ/μ(variance divided by mean) is rather small. For the experimental data examined, σ/μ is typically 0.1 or less (with a few exceptions). For VLSI circuits σ/μ should be even less, as there will be more convergence towards the average value. The situations where σ/μ may not be small are possibly (1) very low level integration devices, (2) very few vectors, and (3) highly regular structures (like memories) with highly regular signal values.

The fact that the total normal chip conductance values under all vectors are about the same has a very important consequence as we shall see below.

From the available experimental data, it can be seen that the excessive supply current values, when any leaky transistors are sensitized, can be easily spotted by inspection (or by using simple algorithms if the process was automated). For the five devices the number of transistors vary in the range from 62 to 432.

The following important question can be asked. Can the effect of a faulty transistor be spotted in a higher integration chip, say, with 10,000 or more transistors? The following is a very rough analysis.

Let the appropriate average conductance for a device be n units (G) and let the average normal per transistor conductance be C. Then under any vector, the measured conductance value will be close to n x C. If we assume that under different vectors, the supply current (and hence the measured conductance) varies by up to 15%, the total normal conductance will be within n x C $\pm$ 15%. Now if the minimum abnormal conductance is C_a, it can cause a measured conductance of n x C $\pm$ 15% + C_a. The abnormal conductance will be apparent by inspection if

$$C_a > C \times n \times \frac{15}{100}$$

or

$$n < \frac{C_a}{C_n} \times \frac{100}{15}$$

If $C_n = 10^{-12}$ ohm^{-1}, $C_a = 10^{-8}$ ohm^{-1}, then

$$n < \frac{10^{-8}}{10^{-12}} \times \frac{100}{15}$$

or

$$n < 6.66 \times 10^4.$$

A n is typically (according to data we have) 30-40% of the number of transistors, in this example resolution will be obtained if

$$\text{number of transistors} < 6.66 \times 10^4 \times \frac{100}{35}$$

$$< 1.90 \times 10^5.$$

This, of course, was a very rough calculation. The numbers would obviously vary for different states of technology.

REFERENCES

[8.1] M. Ostrowski, "Digital Microcircuit Characterization and Specification," General Electric Company Report for Rome Air Development Center, August 1975

IX. CONCLUSIONS

This was necessarily a preliminary study. The basic question posed was - can CMOS devices have additional testability by using leakage testing? The results obtained in this study indicate a positive answer. However, further work is necessary before formal, directly applicable methodology for test generation and information extraction can be obtained.

One constraint this study faced was the lack of up to date and extensive data. The five devices studied in the GE report were of middle 1970's vintage. Technology has since then progressed significantly, and a look should be taken at the newer devices. The five devices were not examined for all possible vectors. This would in fact be nearly impossible for devices with large internal storage. Still, it may be noted that for CD4040A and CD4042A only 4 and 3 vectors, respectively, were used. It was enough for the objectives of the GE report, but not for this study. We were, however, able to obtain very useful insight into the problem, and the data available had been valuable.

Information extraction by using equation-solving approach appears to be of only limited promise. The main problem is not the possible size of set of equations. The fact that the number of independent equations may be smaller than the number of variables can also be partially overcome by use of optimization-type techniques. The real problem is the existence of non-linear terms, which we feel would be very difficult to solve.

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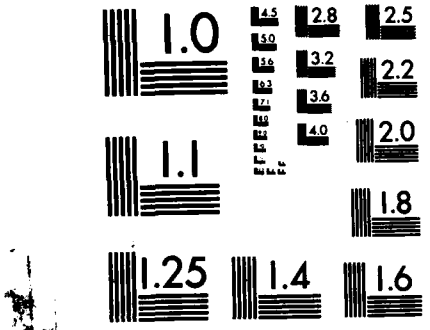

Set-theoretic informatic extraction was considered only for some very simple cases. This is a very powerful approach and should be investigated. It will require only a moderate amount of compution. For devices with lower levels of integration (lower LSI level) it should be straightforward to use. To study the resolution, data for current technology will have to be obtained. The data we analyzed shows, very significantly, a gap of about 3 orders of magnitude between the normal and abnormal leakage curves. This suggests that good resolution can be obtained.

A very significant result of this study was that a relationship between stuck-at 0 and 1 testing and leakage testing exists. It also exists for stuck-on, stuck-open testing.

Some shorted transistors, which cannot be tested by ordinary logical testing, can be easily tested by leakage testing. Leakage testing is also very effective for detecting shorts, although short faults were not examined in detail in this study.

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